Advantech

AQD-D5V32GN48-SB
Datasheet

Rev. 1.0

2022-05-23

Description

AQD-D5V32GN48-SB is DDR5-4800(CL40)-39-39 SDRAM memory module. The SPD is programmed to JEDEC standard latency 4800Mbps timing of 40-39-39 at 1.1V. The module is composed of 16Gb CMOS DDR5 SDRAMs in FBGA package and one 8Kbit SPD Hub in 8pin TDFN package on a 288pin glass–epoxy printed circuit board.

The module is a Dual In-line Memory Module and intended for mounting onto 288 pins edge connector sockets. Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges of DQS. Range of operating frequencies, programmable latencies and burst lengths allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

Features

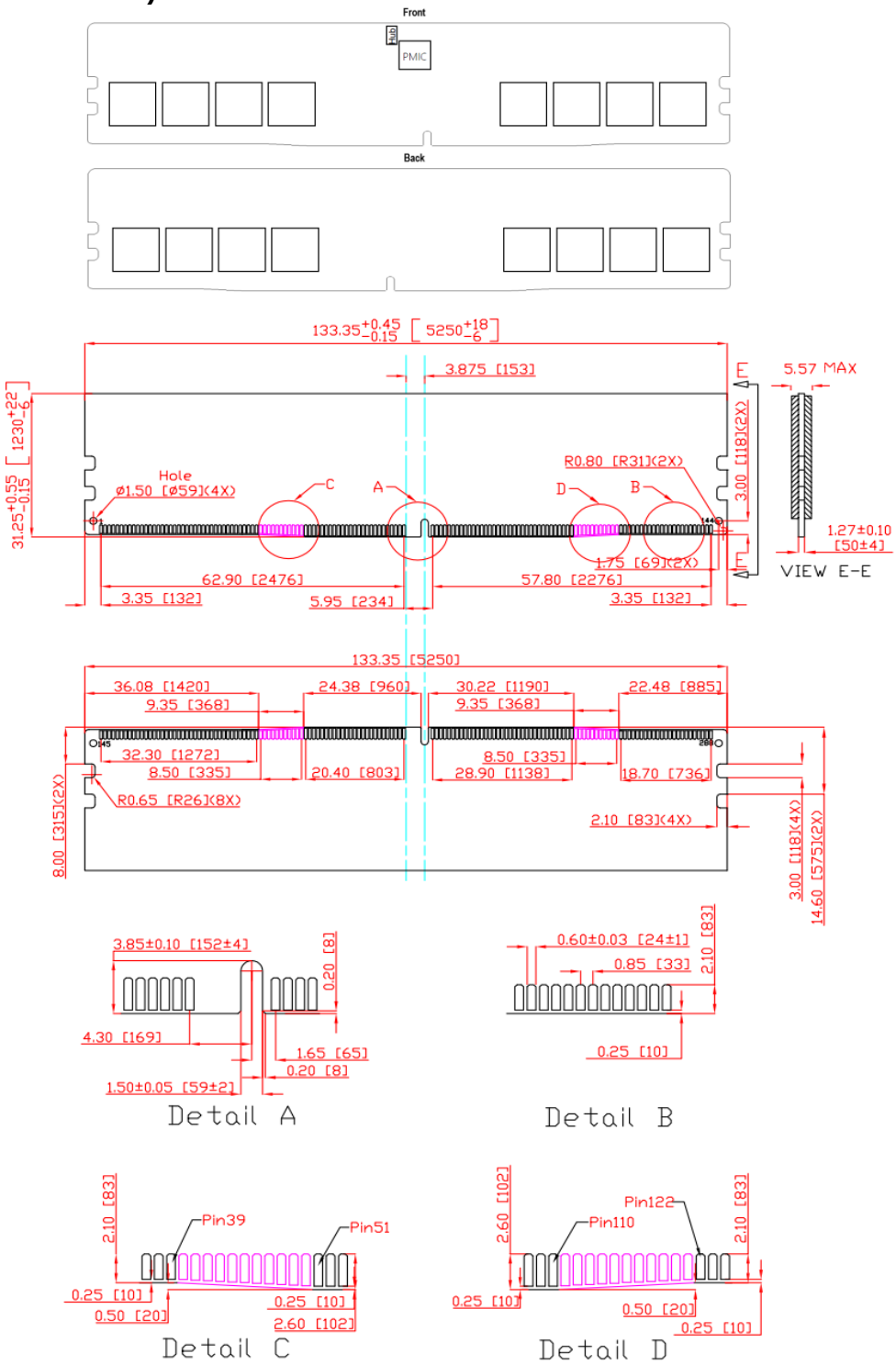
- RoHS compliant products.
- JEDEC standard 1.1V(1.067V~1.166V) Power supply
- VDDQ= 1.1V(1.067V~1.166V)
- VPP = 1.8V(+0.108V / -0.054V)
- Data transfer rates: PC5-4800
- Programmable CAS Latency:22,26,28,30,32,36,40,42
- 16 bit pre-fetch
- Burst Length (BL) switch on-the-fly BL16 or BC8
- Bi-directional Differential Data-Strobe
- On Die Termination, Nominal, Park
- Serial presence detect hub (SPD Hub) with Integrated Temperature sensor
- Asynchronous reset
- PCB edge connector treated with 3u” Gold-Plating

Pin Descriptions

Pin Name	Description		Pin Name	Description
CA[6:0]_A CA[6:0]_B	Address and Command Bus		DQ[31:0]_A DQ[31:0]_B	DIMM memory Data bus channel A & B
CS[1:0]_A CS[1:0]_B	Chip Select		CB[7:0]_A CB[7:0]_B	DIMM ECC Checkbits (CB) channel A & B
PAR_A PAR_B	Parity input		DQS[9:0]_A_t DQS[9:0]_B_t	Data Strobes (positive line of differential pair)
CK_t	Clocks (true/positive)		DQS[9:0]_A_c DQS[9:0]_B_c	Data Strobes (negative line of differential pair)
CK_c	Clocks (complement/negative)		TDQS[9:5]_A_t TDQS[9:5]_B_t	Not valid for x4 operation. Enabled via Mode Register.
ALERT_n	Alert for CRC error		TDQS[9:5]_A_c TDQS[9:5]_B_c	Not valid for x4 operation. Enabled via Mode Register.
RESET_n	Set DRAM to known state		VIN_BULK	DIMM Power Supply from system to PMIC
PCAMP	Control and Monitor Port		VIN_MGMT	DIMM Power Supply from system to PMIC
HSCL	I2C/I3C-Basic Host Sideband Bus Clock		VSS	Power supply return (ground)
HSDA	I2C/I3C-Basic Host Sideband Bus Data		RFU	Reserved for future use
HSA	I2C/I3C-Basic Host Sideband Bus Address		LBDQS	Loopback Data strobe output
LBDQ	Loopback Data output:			

1. TDQSx and DQSx_t share a pin..

Dimensions (Unit: millimeter)



Note:1. Tolerances on all dimensions +/-0.15mm unless otherwise specified.

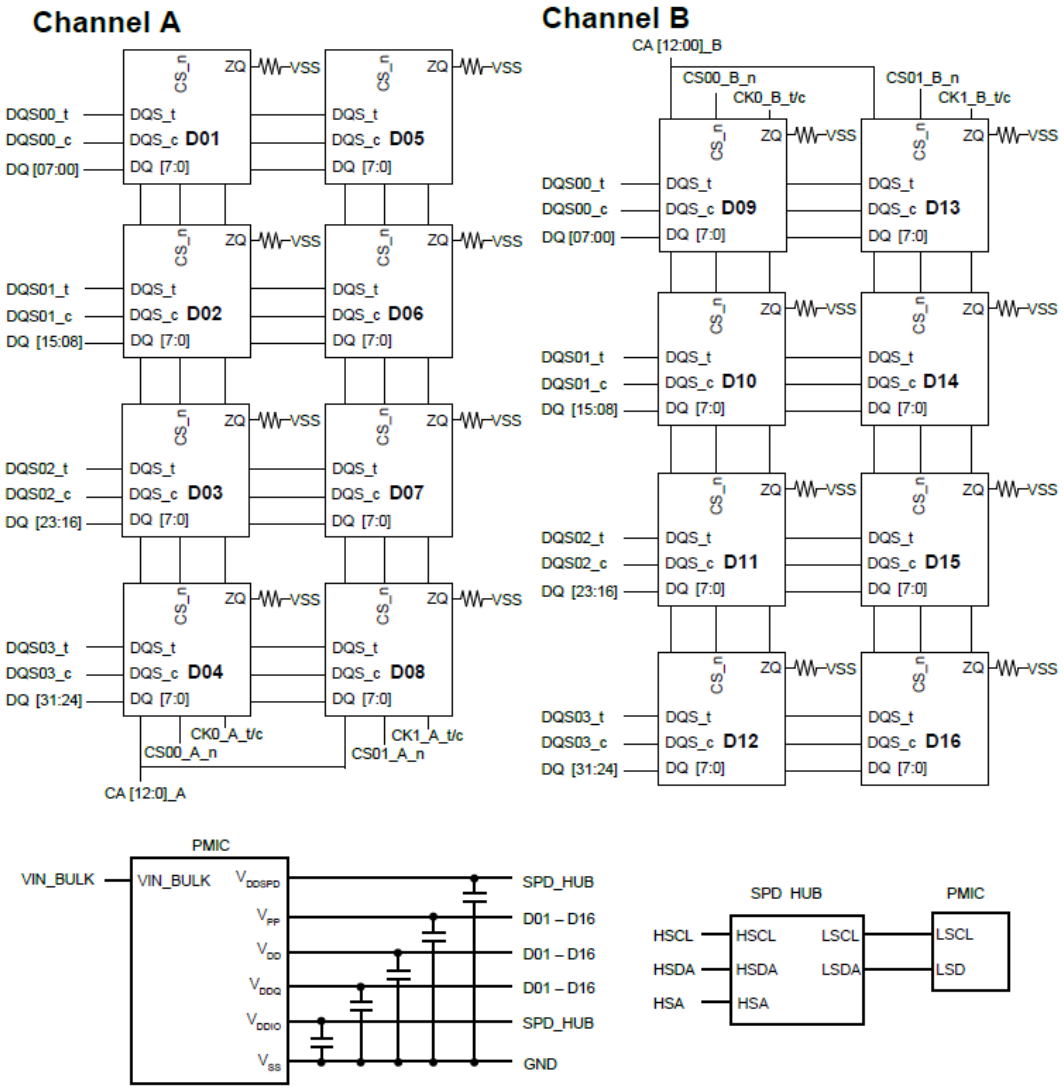
Pin Assignments

288-Pin DDR5 UDIMM Front							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	VIN_BULK	37	DQ20_A	73	CK0_A_c	109	V_{SS}
2	RFU	38	V_{SS}	74	V_{SS}	110	DQ5_B
3	RFU	39	DQ21_A	75	RFU	111	V_{SS}
4	HSCL	40	V_{SS}	76	RFU	112	DQ8_B
5	HSDA	41	DQ24_A	77	V_{SS}	113	V_{SS}
6	V_{SS}	42	V_{SS}	78	CK0_B_t	114	DQ9_B
7	RFU	43	DQ25_A	79	CK0_B_c	115	V_{SS}
8	V_{SS}	44	V_{SS}	80	V_{SS}	116	DM1_B_n
9	DQ0_A	45	DM3_A_n	81	RFU	117	V_{SS}
10	V_{SS}	46	V_{SS}	82	CA12_B	118	DQ12_B
11	DQ1_A	47	DQ28_A	83	V_{SS}	119	V_{SS}
12	V_{SS}	48	V_{SS}	84	CA10_B	120	DQ13_B
13	DQS0_A_c	49	DQ29_A	85	CA8_B	121	V_{SS}
14	DQS0_A_t	50	V_{SS}	86	V_{SS}	122	DQ16_B
15	V_{SS}	51	CB0_A	87	CA6_B	123	V_{SS}
16	DQ4_A	52	V_{SS}	88	CA4_B	124	DQ17_B
17	V_{SS}	53	CB1_A	89	V_{SS}	125	V_{SS}
18	DQ5_A	54	V_{SS}	90	CA2_B	126	DQS2_B_c
19	V_{SS}	55	DQS4_A_c	91	CA0_B	127	DQS2_B_t
20	DQ8_A	56	DQS4_A_t	92	V_{SS}	128	V_{SS}
21	V_{SS}	57	V_{SS}	93	CS0_B_n	129	DQ20_B
22	DQ9_A	58	CS0_A_n	94	V_{SS}	130	V_{SS}
23	V_{SS}	59	V_{SS}	95	RESET_n	131	DQ21_B
24	DM1_A_n	60	CA0_A	96	V_{SS}	132	V_{SS}
25	V_{SS}	61	CA2_A	97	CB0_B	133	DQ24_B
26	DQ12_A	62	V_{SS}	98	V_{SS}	134	V_{SS}
27	V_{SS}	63	CA4_A	99	CB1_B	135	DQ25_B
28	DQ13_A	64	CA6_A	100	V_{SS}	136	V_{SS}
29	V_{SS}	65	V_{SS}	101	DQ0_B	137	DM3_B_n
30	DQ16_A	66	CA8_A	102	V_{SS}	138	V_{SS}
31	V_{SS}	67	CA10_A	103	DQ1_B	139	DQ28_B
32	DQ17_A	68	V_{SS}	104	V_{SS}	140	V_{SS}
33	V_{SS}	69	CA12_A	105	DQS0_B_c	141	DQ29_B
34	DQS2_A_c	70	RFU	106	DQS0_B_t	142	V_{SS}
35	DQS2_A_t	71	V_{SS}	107	V_{SS}	143	RFU
36	V_{SS}	72	CK0_A_t	108	DQ4_B	144	RFU

288-Pin DDR5 UDIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
145	VIN_BULK	181	DQ22_A	217	CK1_A_c	253	V_{SS}
146	VIN_BULK	182	V_{SS}	218	V_{SS}	254	DQ7_B
147	PWR_GOOD	183	DQ23_A	219	RFU	255	V_{SS}
148	HSA	184	V_{SS}	220	RFU	256	DQ10_B
149	RFU	185	DQ26_A	221	V_{SS}	257	V_{SS}
150	V_{SS}	186	V_{SS}	222	CK1_B_t	258	DQ11_B
151	PWR_EN	187	DQ27_A	223	CK1_B_c	259	V_{SS}
152	RFU	188	V_{SS}	224	V_{SS}	260	DQS1_B_c
153	V_{SS}	189	DQS3_A_c	225	RFU	261	DQS1_B_t
154	DQ2_A	190	DQS3_A_t	226	RFU	262	V_{SS}
155	V_{SS}	191	V_{SS}	227	V_{SS}	263	DQ14_B
156	DQ3_A	192	DQ30_A	228	CA11_B	264	V_{SS}
157	V_{SS}	193	V_{SS}	229	CA9_B	265	DQ15_B
158	DM0_A_n	194	DQ31_A	230	V_{SS}	266	V_{SS}
159	V_{SS}	195	V_{SS}	231	CA7_B	267	DQ18_B
160	DQ6_A	196	CB2_A	232	CA5_B	268	V_{SS}
161	V_{SS}	197	V_{SS}	233	V_{SS}	269	DQ19_B
162	DQ7_A	198	CB3_A	234	CA3_B	270	V_{SS}
163	V_{SS}	199	V_{SS}	235	CA1_B	271	DM2_B_n
164	DQ10_A	200	ALERT_n	236	V_{SS}	272	V_{SS}
165	V_{SS}	201	V_{SS}	237	CS1_B_n	273	DQ22_B
166	DQ11_A	202	CS1_A_n	238	V_{SS}	274	V_{SS}
167	V_{SS}	203	V_{SS}	239	DQS4_B_c	275	DQ23_B
168	DQS1_A_c	204	CA1_A	240	DQS4_B_t	276	V_{SS}
169	DQS1_A_t	205	CA3_A	241	V_{SS}	277	DQ26_B
170	V_{SS}	206	V_{SS}	242	CB2_B	278	V_{SS}
171	DQ14_A	207	CA5_A	243	V_{SS}	279	DQ27_B
172	V_{SS}	208	CA7_A	244	CB3_B	280	V_{SS}
173	DQ15_A	209	V_{SS}	245	V_{SS}	281	DQS3_B_c
174	V_{SS}	210	CA9_A	246	DQ2_B	282	DQS3_B_t
175	DQ18_A	211	CA11_A	247	V_{SS}	283	V_{SS}
176	V_{SS}	212	V_{SS}	248	DQ3_B	284	DQ30_B
177	DQ19_A	213	RFU	249	V_{SS}	285	V_{SS}
178	V_{SS}	214	RFU	250	DM0_B_n	286	DQ31_B
179	DM2_A_n	215	V_{SS}	251	V_{SS}	287	V_{SS}
180	V_{SS}	216	CK1_A_t	252	DQ6_B	288	RFU

Function Block Diagram

2Rank, x8 DDR5 SDRAMs



Note 1: ZQ resistors are 240 Ω ± 1%.

Operating Temperature Condition

Parameter	Symbol	Rating	Unit	Note
Operating Temperature	TOPER	0 to 85	°C	1,2

Note: Operating Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

Absolute Maximum DC Ratings

Parameter	Symbol	Value	Unit	Note
Voltage on V_{DD} relative to Vss	VDD	-0.3 ~ 1.4	V	1
Voltage on V_{DDQ} pin relative to Vss	VDDQ	-0.3 ~ 1.4	V	1
Voltage on any pin relative to Vss	VIN, VOUT	-0.3 ~ 1.4	V	1
Storage temperature	T_{STG}	-55~+100	°C	1,2

Note:
1. Stress greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

AC & DC Operating Conditions

Recommended DC operating conditions

Parameter	Symbol	Voltage	Rating			Unit	Notes
			Min	Typ.	Max		
Host Supply Voltage	VIN_BULK	12.0	4.25	5.0	5.5	V	
PMIC Output Supply Voltage	VDD	1.1	1.067	1.1	1.166	V	1,2,3
PMIC Output Supply Voltage	VDDQ	1.1	1.067	1.1	1.166	V	1,2,3
PMIC Output Supply Voltage	VPP	1.8	1.746	1.8	1,908	V	3
AC Input Logic High	$V_{IH(AC)}$	TBD	-	-	-	mV	
AC Input Logic Low	$V_{IL(AC)}$	TBD	-	-	-	mV	
DC Input Logic High	$V_{IH(DC)}$	TBD	-	-	-	mV	
DC Input Logic Low	$V_{IL(DC)}$	TBD	-	-	-	mV	

Note: (1) VDD must be within 66mv of VDDQ
(2) AC parameters are measured with VDD and VDDQ tied together.
(3) This includes all voltage noise from DC to 2 MHz at the DRAM package ball.

IDD Specification parameters Definition - 32GB

Symbol	Condition	32GB	Unit
IDD0	One bank ACTIVATE-PRECHARGE current	608	mA
IDD0F	Operating Four Bank Active-Precharge Current	984	mA
IDD2N	Precharge Standby Current	480	mA
IDD2P	Precharge Power-Down Current	368	mA
IDD3N	Active standby current	80	mA
IDD3P	Active Power-Down Current	480	mA
IDD4R	Burst Read Current	1704	mA
IDD4W	Burst write current	2024	mA
IDD5B	Burst Refresh Current (1x REF)	2024	mA
IDD5C	Burst Refresh Current (Same Bank Refresh Mode)	992	mA
IDD6N	Self refresh current: Normal temperature range (0–85°C)	2744	mA
IDD7	Bank interleave read current	256	mA
IDD8	Maximum power-down current	608	mA

■ Timing Parameters & Specifications

Parameter	Symbol	DDR5-4400		DDR5-4800		DDR5-5200		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Clock Timing									
Clock period average	tCK (AVG)	0.5	<0.500	0.4	<0.454	0.4	<0.416	ns	1
Command and Address Timing									
Read to Read command delay for same bank group	tCCD_L	max(8nCK, 5ns)	–	max(8nCK, 5ns)	–	max(8nCK, 5ns)	–	nCK,ns	
Write to Write command delay for same bank groupp	tCCD_L_WR	max(32nCK, 20ns)	–	max(32nCK, 20ns)	–	max(32nCK, 20ns)	–	nCK,ns	
Write to Write command delay for same bank group, second write not RMW	tCCD_L_WR2	max(16nCK, 10ns)	–	max(16nCK, 10ns)	–	max(16nCK, 10ns)	–	nCK,ns	
Read to Write command delay for same bank group	tCCD_L_RTW	CL - CWL + RBL/2 + 2tCK - (Read DQS offset) + (tRPST - 0.5tCK) + tWPRE						nCK,ns	3,5,6
Write to Read command delay for same bank group	tCCD_L_WTR	CWL + WBL/2 + Max(16nCK,10ns)						nCK,ns	4,6
Read to Read command delay for different bank group	tCCD_S	8	–	8	–	8	–	nCK	
Write to Write command delay for different bank group	tCCD_S_WR	8	–	8	–	8	–	nCK	
Read to Write command delay for different bank group	tCCD_S_RTW	CL - CWL + RBL/2 + 2tCK - (Read DQS offset) + (tRPST - 0.5tCK) + tWPRE						nCK,ns	3,5,6
Write to Read command delay for different bank group	tCCD_S_WTR	CWL + WBL/2 + Max(4nCK,2.5ns)						nCK,ns	4,6
Write to Read with Auto Precharge command delay for same bank	tCCD_WTRA	CWL + WBL/2 + tWR - tRTP						nCK,ns	2,4,6

Parameter	Symbol	DDR5-4400		DDR5-4800		DDR5-5200		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Activate to Activate command delay to same bank group for 1KB page size	tRRD_L(1K)	max(8nCK, 5ns)	–	max(8nCK, 5ns)	–	max(8nCK, 5ns)	–	nCK,ns	
Activate to Activate command delay to same bank group for 2KB page size	tRRD_L(2K)	max(8nCK, 5ns)	–	max(8nCK, 5ns)	–	max(8nCK, 5ns)	–	nCK,ns	
Activate to Activate command delay to different bank group for 1KB page size	tRRD_S(1K)	8	–	8	–	8	–	nCK	
Activate to Activate command delay to different bank group for 2KB page size	tRRD_S(2K)	8	–	8	–	8	–	nCK	
Four activate window for 1KB page size	tFAW (1K)	Max(32nCK, 14.545ns)	–	Max(32nCK, 13.333ns)	–	Max(32nCK, 12.307ns)	–	nCK,ns	
Four activate window for 2KB page size	tFAW (2K)	Max(40nCK, 18.181ns)	–	Max(40nCK, 16.666ns)	–	Max(40nCK, 15.384ns)	–	nCK,ns	
Read to Precharge command delay	tRTP	Max(12nCK, 7.5ns)	–	Max(12nCK, 7.5ns)	–	Max(12nCK, 7.5ns)	–	nCK,ns	
Precharge to Precharge command delay	tPPD	2	–	2	–	2	–	nCK	7
Write recovery time	tWR	30	–	30	–	30	–	ns	

Notes:

1. tCK(avg)min listed for reference only, refer to the Speed Bins and Operations section which lists all valid tCK(avg) values.

2. tCCD_WTRA(min) shall always be greater than or equal to CWL + WBL/2 + tWR(min) - tRTP(min), and when using the appropriate rounding algorithms,

   nCCD_WTRA(min) shall always be greater than or equal to CWL + WBL/2 + nWR(min) - nRTP(min).

3. RBL: Read burst length associated with Read command

   RBL = 32 (36 w/ RCRC on) for fixed BL32 and BL32 in BL32 OTF mode

   RBL = 16 (18 w/ RCRC on) for fixed BL16 and BL16 in BL32 OTF mode

   RBL = 16 (18 w/ RCRC on) for BL16 in BC8 OTF mode and BC8 in BC8 OTF mode

4. WBL: Write burst length associated with Write command

   WBL = 32 (36 w/ WCRC on) for fixed BL32 and BL32 in BL32 OTF mode

   WBL = 16 (18 w/ WCRC on) for fixed BL16 and BL16 in BL32 OTF mode

   WBL = 16 (18 w/ WCRC on) for BL16 in BC8 OTF mode and BC8 in BC8 OTF mode

5. 5 - The following is considered for tRTW equation

   1tCK needs to be added due to tDQS2CK

   Read DQS offset timing can pull in the tRTW timing

   1tCK needs to be added when 1.5tCK postamble

6. CWL=CL-2

7. tPPD applies to any combination of precharge commands (PREab, PREsb, PREpb). tPPD also applies to any combination of precharge commands to a different die in a 3DS DDR5 SDRAM.

SERIAL PRESENCE DETECT SPECIFICATION

Byte	Function Described	Function		HEX Value
0	Number of Bytes in SPD Device	SPD Total: 1024Bytes		30
1	SPD Revision for Base Configuration Parameters	Version 1.0		10
2	Key Byte / Host Bus Command Protocol Type	DDR5 SDRAM		12
3	Key Byte / Module Type	U-DIMM		02
4	First SDRAM Density and Package	Monolithic SDRAM	16Gb	04
5	First SDRAM Addressing	Row : 16	Column : 10	00
6	First SDRAM I/O Width	x8		20
7	First SDRAM Bank Groups & Banks Per Bank Group	8 bank groups/4 banks per bank group		62
8	Second SDRAM Density and Package			00
9	Second SDRAM Addressing			00
10	Secondary SDRAM I/O Width			00
11	Second SDRAM Bank Groups & Banks Per Bank Group			00
12	SDRAM BL32 & Post Package Repair	sPPR Undo/Lock supported	Burst length 32 supported	70
13	SDRAM Duty Cycle Adjuster & Partial Array Self Refresh	PASR/Device supports DCA for 4-phase internal clock(s)		00
14	SDRAM Fault Handling			00
15	Reserved	must be coded as 0x00		00
16	SDRAM Nominal Voltage, VDD	Operable:1.1V	Endurant:1.1V	00
17	SDRAM Nominal Voltage, VDDQ	Operable:1.1V	Endurant:1.1V	00
18	SDRAM Nominal Voltage, VPP	Operable:1.8V	Endurant:1.8V	00
19	SDRAM Timing	Standard core timings per JESD79-5		00
20	SDRAM Minimum Cycle Time (tCKAVGmin), Least Significant Byte	416 ps		A0
21	SDRAM Minimum Cycle Time (tCKAVGmin), Most Significant Byte			01
22	SDRAM Maximum Cycle Time (tCKAVGmax), Least Significant Byte	1010 ps		F2
23	SDRAM Maximum Cycle Time (tCKAVGmax), Most Significant Byte			03
24	SDRAM CAS Latencies Supported:First Byte	CL22,26,28,30,32		7A
25	SDRAM CAS Latencies Supported:Second Byte	CL36,40,42		0D
26	SDRAM CAS Latencies Supported:Third Byte	-		00
27	SDRAM CAS Latencies Supported:Fourth Byte	-		00
28	SDRAM CAS Latencies Supported:Fifth Byte	-		00
29	Reserved	must be coded as 0x00		00
30	SDRAM Minimum CAS Latency Time (tAAmin), Least Significant Byte	16000 ps		80
31	SDRAM Minimum CAS Latency Time (tAAmin), Most Significant Byte			3E
32	SDRAM Minimum RAS to CAS Delay Time (tRCDmin), Least Significant Byte	16000 ps		80
33	SDRAM Minimum RAS to CAS Delay Time (tRCDmin), Most Significant Byte			3E
34	SDRAM Minimum Row Precharge Delay Time (tRPmin), Least Significant Byte	16000 ps		80
35	SDRAM Minimum Row Precharge Delay Time (tRPmin), Most Significant Byte			3E
36	SDRAM Minimum Active to Precharge Delay Time (tRASmin), Least Significant Nibble	32000 ps		00
37	SDRAM Minimum Active to Precharge Delay Time (tRASmin), Most Significant Byte			7D
38	SDRAM Minimum Active to Active/Refresh Delay Time (tRCmin), Least Significant Nibble	48000 ps		80
39	SDRAM Minimum Active to Active/Refresh Delay Time (tRCmin), Most Significant Nibble			BB
40	SDRAM Minimum Write Recovery Time (tWRmin), Least Significant Nibble	30000 ps		30
41	SDRAM Minimum Write Recovery Time (tWRmin), Most Significant Nibble			75
42	SDRAM Minimum Refresh Recovery Delay Time (tRFC1min, tRFC1_slr min),Least Significant Byte	295 ns		27
43	SDRAM Minimum Refresh Recovery Delay Time (tRFC1min, tRFC1_slr min),Most Significant Byte			01
44	SDRAM Minimum Refresh Recovery Delay Time (tRFC2min, tRFC2_slr min),Least Significant Byte	160 ns		A0
45	SDRAM Minimum Refresh Recovery Delay Time (tRFC2min, tRFC2_slr min),Most Significant Byte			00
46	SDRAM Minimum Refresh Recovery Delay Time (tRFCsbmin, tRFCsb_slr min),Least Significant Byte	130 ns		82
47	SDRAM Minimum Refresh Recovery Delay Time (tRFCsbmin, tRFCsb_slr min),Most Significant Byte			00
48	SDRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank(tRFC1_dlr min),Least Significant Byte	monolithic SDRAMs		00
49	SDRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank(tRFC1_dlr min),Most Significant Byte			00
50	SDRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank(tRFC2_dlr min),Least Significant Byte	monolithic SDRAMs		00
51	SDRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank(tRFC2_dlr min),Most Significant Byte			00
52	SDRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank(tRFCsb_dlr min),Least Significant Byte	monolithic SDRAMs		00
53	SDRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank(tRFCsb_dlr min),Most Significant Byte			00
54	SDRAM Refresh Management, First Byte, First SDRAM			00
55	SDRAM Refresh Management, Second Byte, First SDRAM			00
56	SDRAM Refresh Management, First Byte, Second SDRAM			00
57	SDRAM Refresh Management, Second Byte, Second SDRAM			00
58	SDRAM Adaptive Refresh Management, First SDRAM, First Byte,Level A			00
59	SDRAM Adaptive Refresh Management, First SDRAM, Second Byte,Level A			00
60	SDRAM Adaptive Refresh Management, Second SDRAM, First Byte,Level A			00
61	SDRAM Adaptive Refresh Management, Second SDRAM, Second Byte,Level A			00
62	SDRAM Adaptive Refresh Management, First SDRAM, First Byte,Level B			00
63	SDRAM Adaptive Refresh Management, First SDRAM, Second Byte,Level B			00
64	SDRAM Adaptive Refresh Management, Second SDRAM, First Byte,Level B			00

65	SDRAM Adaptive Refresh Management, Second SDRAM, Second Byte,Level B			00
66	SDRAM Adaptive Refresh Management, First SDRAM, First Byte,Level C			00
67	SDRAM Adaptive Refresh Management, First SDRAM, Second Byte,Level C			00
68	SDRAM Adaptive Refresh Management, Second SDRAM, First Byte,Level C			00
69	SDRAM Adaptive Refresh Management, Second SDRAM, Second Byte,Level C			00
70	SDRAM Minimum Active to Active Command Delay Time, Same Bank Group,(tRRD_Lmin),Least Significant Byte	5000	ps	88
71	SDRAM Minimum Active to Active Command Delay Time, Same Bank Group,(tRRD_Lmin),Most Significant Byte			13
72	SDRAM Minimum Active to Active Command Delay Time, Same Bank Group,(tRRD_Lmin),Lower Clock Limit	8	nCK	08
73	SDRAM Minimum CAS_n to CAS_n Command Delay Time, Same Bank Group,(tCCD_Lmin),Least Significant Byte	5000	ps	88
74	SDRAM Minimum CAS_n to CAS_n Command Delay Time, Same Bank Group,(tCCD_Lmin),Most Significant Byte			13
75	SDRAM Minimum CAS_n to CAS_n Command Delay Time, Same Bank Group,(tCCD_Lmin),Lower Clock Limit	8	nCK	08
76	SDRAM Minimum Write CAS_n to Write CAS_n Command Delay Time, Same Bank Group (tCCD_L_WRmin),Least Significant Byte	20000	ps	20
77	SDRAM Minimum Write CAS_n to Write CAS_n Command Delay Time, Same Bank Group (tCCD_L_WRmin),Most Significant Byte			4E
78	SDRAM Minimum Write CAS_n to Write CAS_n Command Delay Time, Same Bank Group (tCCD_L_WRmin),Lower Clock Limit	32	nCK	20
79	SDRAM Minimum Write CAS_n to Write CAS_n Command Delay Time, Same Bank Group (tCCD_L_WR2min),Least Significant Byte	10000	ps	10
80	SDRAM Minimum Write CAS_n to Write CAS_n Command Delay Time, Same Bank Group (tCCD_L_WR2min),Most Significant Byte			27
81	SDRAM Minimum Write CAS_n to Write CAS_n Command Delay Time, Same Bank Group (tCCD_L_WR2min),Lower Clock Limit	16	nCK	10
82	SDRAM Minimum Four Activate Window (tFAWmin),Least Significant Byte	13333	ps	15
83	SDRAM Minimum Four Activate Window (tFAWmin),Most Significant Byte			34
84	SDRAM Minimum Four Activate Window (tFAWmin),Lower Clock Limit	32	nCK	20
85	SDRAM Write to Read Command Delay for Same Bank Group (tCCD_L_WTR),Least Significant Byte	10000	ps	10
86	SDRAM Write to Read Command Delay for Same Bank Group (tCCD_L_WTR), Most Significant Byte			27
87	SDRAM Write to Read Command Delay for Same Bank Group (tCCD_L_WTR),Lower Clock Limit	16	nCK	10
88	SDRAM Write to Read Command Delay for Different Bank Group (tCCD_S_WTR), Least Significant Byte	2500	ps	C4
89	SDRAM Write to Read Command Delay for Different Bank Group (tCCD_S_WTR), Most Significant Byte			09
90	SDRAM Write to Read Command Delay for Different Bank Group,(tCCD_S_WTR), Lower Clock Limit	4	nCK	04
91	SDRAM Read to Precharge Command Delay (tRTP, tRTP_slr), Least Significant Byte	7500	4A	4C
92	SDRAM Read to Precharge Command Delay (tRTP, tRTP_slr), Most Significant Byte			1D
93	SDRAM Read to Precharge Command Delay (tRTP, tRTP_slr), Lower Clock Limit	12	nCK	0C
94-127	Reserved, Base Configuration Section	Must be coded as 0x00		00
128-191	Reserved for future use	Reserved for future use		00
192	SPD Revision for Module Information	Version 1.0		10
193	Hashing Sequence	No authentication		00
194	SPD Manufacturer ID Code, First Byte	By SPD_Hub & PMIC Vendor & Revision *Note: 1		-
195	SPD Manufacturer ID Code, Second Byte			-
196	SPD Device Type			-
197	SPD Device Revision Number			-
198	PMIC 0 Manufacturer ID Code, First Byte			-
199	PMIC 0 Manufacturer ID Code, Second Byte			-
200	PMIC 0 Device Type			-
201	PMIC 0 Revision Number			-
202	PMIC 1 Manufacturer ID Code, First Byte			00
203	PMIC 1 Manufacturer ID Code, Second Byte			00
204	PMIC 1 Device Type			00
205	PMIC 1 Revision Number			00
206	PMIC 2 Manufacturer ID Code, First Byte			00
207	PMIC 2 Manufacturer ID Code, Second Byte			00
208	PMIC 2 Device Type			00
209	PMIC 2 Revision Number			00
210	Thermal Sensor Manufacturer ID Code, First Byte			00
211	Thermal Sensor Manufacturer ID Code, Second Byte			00
212	Thermal Sensor Device Type			00
213	Thermal Sensor Revision Number			00
214	DRAM Specification Level			00
215	SPD Specification Level			00
216	PMIC0 Specification Level			00
217	PMIC1 Specification Level			00
218	PMIC2 Specification Level			00
219	TS Specification Level			00
220	DIMM Specification Level			00
221-229	Reserved	Reserved		00
230	(Unbuffered): Module Nominal Height	31.25mm		11
231	(Unbuffered): Module Maximum Thickness	Front,Back,1 < thickness < 2 mm		11
232	(Unbuffered): Reference Raw Card Used	Raw Card B	Revision 0	01
233	(Unbuffered): DIMM Attributes	0 to +95 °C/1 row DRAM		81
234	(Unbuffered): Module Organization	2 Package Ranks		08
235	Memory Channel Bus Width	2 channels/32 bits		22
236-239	Reserved	must be coded as 0x00		00
240~447	(Unbuffered):Module Type Specific Information	Reserved		00

448-509	Reserved for future use	-	**00**
510	CRC for Byte 0~509,Least Significant Byte	**CRC**	**-**
511	CRC for Byte 0~509,Most Significant Byte	**CRC**	**-**
512	Module Manufacturer ID Code, First Byte		**04**
513	Module Manufacturer ID Code, Second Byte		**CB**
514	Module Manufacturing Location	*Note: 2	**-**
515	Module Manufacturing Date	*Note: 3 (Decimal)	**-**
516	Module Manufacturing Date	*Note: 4 (Decimal)	**-**
517	Module Serial Number	*Note: 5 (Decimal)	**-**
518			**-**
519			**-**
520			**-**
521~550	Module Part Number	*Note: 6	**--**
551	Module Revision Code		**00**
552	DRAM Manufacturer ID Code, First Byte	*Note: 7	**-**
553	*DRAM* Manufacturer ID Code, Second Byte		**-**
554	DRAM Stepping	Undefined/Stepping information not provided	**FF**
555-639	Manufacturer's Specific Data	*Note: 8	**-**
640	Intel Extreme Memory Profile Identification String		**00**
641	Intel Extreme Memory Profile Identification String		**00**
642	Intel Extreme Memory Profile Version		**00**
643	Intel Extreme Memory Profile Organization		**00**
644	Intel Extreme Memory Profile Configuration		**00**
645	PMIC Vendor ID		**00**
646	PMIC Vendor ID		**00**
647	Number of PMICs		**00**
648	PMIC Capabilities		**00**
649-653	RSVD		**00**
654~701	Profile 1/2/3 String Name		**00**
702~895	Profile 1/2/3 Parameter		**00**
896-1023	User Settings		**00**

Note :

1. Byte 194-201 -- By SPD_Hub & PMIC Vendor & Revision
1.1 Byte 194-197 – RENESAS[(0x80), (0xB3), (0x80), (0x21)] ; MONTAGE[(0x86), (0x32), (0x80), (0x15)]
1.2 Byte 198-201 – RENESAS[(0x80), (0xB3), (0x82), (0x20)] ; RICHTEK[(0x8A), (0x8C), (0x82), (0x11)]
2. Byte 514 -- Manufacturing location by manufacturing location
3. Byte 515 -- Module manufacturing date by year (YY). (Decimal)
4. Byte 516 -- Module manufacturing date by week (WW). (Decimal)
5. Bytes 517-520 -- Module Serial Number. (Decimal)
6. Bytes 521-550 -- Module Part Number. (ASCII format, unused digits are coded as ASCII blanks (0x20).
7. Bytes 552-553 -- DRAM Manufacturer ID Code by JEDEC definition. SAMSUNG :[(0x80) ,(0xCE)]
8. Bytes 555~639 -- These bytes are undefined and can be used own purpose.