

AMD NPT Family 0Fh Mobile Processor Power and Thermal Data Sheet

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Revision History

Date	Revision	Description
November 2007	3.40	NDA update release. • Added new OPN AMDTK55HAX4CT in the AMD Athlon™ 64 X2 dual-core section.
September 2007	3.37	NDA update release. • Added new OPN TMDTL68HAX5DM to the AMD Turion™ 64 X2 Mobile Technology Section. • Added new OPN AMDTK57HAX4DM to the Mobile AMD Athlon™ 64 X2 Dual-Core Section. • Added new Embedded section with new OPN SMF2100HAX3DQ. • Revised Part Definition DQ entry in Table 1 on page 14.
August 2007	3.34	NDA update release. • Added new OPNs in the Mobile AMD Sempron™ Processor section. • Upgraded Power and Thermal Table headings.
June 2007	3.30	NDA update release. • Table 8 on page 16, last row (under Revision column) -- changed “F2” to “G2.” • Table 17 on page 32, last row (under CPUID column) -- changed “00070FC2h” to 00060F82h.”
June 2007	3.28	NDA update release. • Added new OPNs in the AMD Turion™ 64 X2 Mobile Technology section. • Added OPNs in the Mobile AMD Sempron™ Processor section.
March 2007	3.26	NDA update release. • Added new OPN in the AMD Turion™ 64 X2 Mobile Technology section. • Added new Section 5.3.2 on page 50 in Chapter 5, with OPN AMDTK53HAX4DC. • Revised IDDC1 Max @ Max P-state, thermal resistance values and S3 IO power for OPNs in the AMD Turion™ 64 X2 Mobile Technology section.
March 2007	3.25	Internal review copy for NDA update release.
March 2007	3.24	Internal review copy for NDA update release.
March 2007	3.23	Internal review copy for NDA update release.
February 2007	3.22	NDA update release. • Revised Adjusted Peak Performance (APP) Calculations.
February 2007	3.20	NDA update release. • Added APP section. • Revised specifications of four OPNs in the AMD Turion™ 64 X2 Mobile Technology section. • Revised VDD_ac power supply note.

Date	Revision	Description
January 2007	3.16	NDA update release. • Added new OPNs to the AMD Turion™ 64 X2 Mobile Technology section. • Revised IDDC1 Max @ Max P-state and IDDC1E values for several OPNs in the AMD Turion™ 64 X2 Mobile Technology section. • Revised the power limit encodings in Table 49 on page 68 and in Table 50 on page 69. • Updated some values for the OPNs in Section 4.3.2, TMD mmmsvtc DC Thermal and Power Specifications on p. 32 and p. 33.
December 2006	3.11	NDA update release. • Added new voltage options to 25W Mobile AMD Sempron™ Processor OPNs. • Added new 35W Mobile AMD Sempron™ Processor OPN. • Added new OPN to the AMD Turion™ 64 Mobile Technology section. • Revised IDDC1 Max @ Max P-State, IDDC1 Max @ Min P-State and IDDC3 Max for several OPNs in all sections.
October 2006	3.07	Added one voltage to the MK36 model part. Updated Table 49. Socket AM2 Processor Power Limit Encoding.
September 2006	3.05	Added new voltage option to OPN TMDMK36HAX4CM. Added new power limit encodings.
September 2006	3.03	Added new part to Section 4.3.1, on page 37, with the OPN TMDTL64HAX5CT and removed OPN AMN4600IAT5CU
August 2006	3.01	Added new Section 3 AMD Turion™ 64 Mobile Technology on page 25. Revised note 9 in Section 4.3.1 on page 36.
July 2006	2.10	Added mobile AMD Sempron™ processor part and AMD Athlon™ 64 X2 dual-core processor part.
June 2006	2.08	Added new Section 5 AMD Athlon™ 64 X2 Dual-Core Processor on page 44 with OPNs AMN3800IAT5CU and AMN4200IAT5CU; updated OPN tables. Removed Socket F (1207) data.
March 2006	2.06	Updated power values for all parts. Added package drawing references.
February 2006	2.04	Brand name “Turion” changed to “Turion X2”. Added Section 9 on page 70 MTOPS.
February 2006	2.02	Initial NDA release.

1 Overview

This document contains processor thermal specifications and power specifications. The specifications in this document supersede those found in the power roadmaps. For all other electrical specifications, refer to the appropriate product data sheet and the *AMD NPT Family 0Fh Processor Electrical Data Sheet,* order #31119.

1.1 Organization

This document is organized into the following sections:

- Document overview (Section 1)
- One section for each brand represented in the mobile segment containing the following subsections:
  - Ordering part number (OPN) description (content overview in Section 1.1.1)
  - Thermal and power specification tables (content overview in Section 1.1.3 on page 11)
- Power supply specifications (content overview in Section 1.1.4 on page 11)
- Power limit encoding specifications (content overview in Section 1.1.5 on page 11)
- MTOPS section on page 70.

1.1.1 Ordering Part Number Description Section Overview

The Ordering Part Number (OPN) Description section contains a depiction and description of a valid OPN for the brand contained in that chapter. Each character or group of characters within an OPN has a specific meaning (for example, model number, socket compatibility). The meaning of each OPN character is detailed in the OPN description section. Each OPN identifies a processor with a unique thermal and power specification table entry.

The OPN description section also contains a full description of the Subsection Ordering Part Number (SOPN) abstraction characters for the brand contained in that chapter. SOPNs are used to group and organize OPNs into subsections for the thermal and power tables and power supply specifications. A definition of SOPNs is contained in Section 1.3 on page 12.

1.1.2 Thermal and Power Table Guide Overview

The thermal and power table guide section contains a table mapping SOPNs and the properties associated with their defined characters to the proper thermal and power table subsections and page numbers. This table is designed to be used as a quick reference for finding the appropriate subsection for the thermal and power tables corresponding to an SOPN.

1.1.3 Thermal and Power Table Section Overview

The thermal and power specification tables contain the thermal and power requirements for each OPN. This includes the information necessary for thermal management (for example, heat sink requirements, ambient temperature assumptions) and power delivery (for example, voltage and current, and power dissipation for each P-state).

The thermal and power specification tables are organized into subsections that correspond to Subsection Ordering Part Numbers (SOPNs). SOPNs for the thermal and power tables have the brand, power limit, and part definition characters defined. They are of the form **ABC** mmmmsvtc **GH**. Each chapter provides a guide table that maps the SOPNs in the thermal and power tables within that chapter to the appropriate subsection number and page number. Within each subsection the OPNs are sorted by model number, socket compatibility, voltage, temperature, and cache size, respectively.

1.1.4 Power Supply Specification Chapter Overview

The power supply specification chapter contains the operating conditions and requirements for all voltage planes required by the processor. Power supply requirements are organized into subsections that correspond to SOPNs. SOPNs for the power supply specifications have the socket compatibility character defined. They are of the form ispmmmm**S**vtcdd.

1.1.5 Power Limit Encoding Chapter Overview

A power limit is encoded into each processor. The power limit encoding section defines these encodings and their interpretation. Refer to the *BIOS and Kernel Developer's Guide for AMD NPT Family 0Fh Processors*, order #32559, for details on BIOS usage of the power limit encoding.

1.2 Conventions

Following are conventions used with numbers.

- Binary numbers. Binary numbers are indicated by appending a "b" at the end, for example: 0110b.
- Decimal numbers. Unless specified otherwise, all numbers are decimal.
- Hexadecimal numbers. Hexadecimal numbers are indicated by appending an "h" to the end, for example: 45F8h.
- Underscores in numbers. Underscores are used to break up numbers to make them more readable, for example: 0110_1100b. They do not imply any operation.

1.3 Definitions

Following are some key definitions.

- **OPN**. Ordering Part Number. An OPN uniquely identifies a processor and its associated specifications in the thermal and power tables and power supply specifications section.
- **P-state**. Processor Performance State. P-states are valid combinations of processor voltage and frequency.
- **SOPN**. Subsection Ordering Part Number. An SOPN is an OPN with a subset of defined characters. All defined characters in an SOPN are bolded and capitalized. All abstracted characters in an SOPN are in non-bolded lowercase. Information for any OPN that matches all of the defined characters in an SOPN is contained in that subsection. For example, OPN ABC123DEF5GH appears under the subsection for SOPN **ABC**mmmmstvc**GH**. The abstracted (lowercase) character definitions for SOPNs are contained in the OPN description section of each chapter.
- **TDP**. Thermal Design Power. The thermal design power is the maximum power a processor can draw for a thermally significant period while running commercially useful software. The constraining conditions for TDP are specified in the notes in the thermal and power tables.
- **VID_VDD**. The VID_VDD voltage is the VID[5:0] requested VDD supply level. Refer to the *BIOS and Kernel Developer's Guide for AMD NPT Family 0Fh Processors*, order #32559, for VID[5:0] to voltage translation specifications.

2 Mobile AMD Sempron™ Processor

The following sections contain the OPN description and thermal and power specifications for the Mobile AMD Sempron™ Processor. Each column in the thermal and power tables represents a specific Ordering Part Number (OPN). Section 2.1 provides an example of the OPN structure for this processor family.

2.1 Mobile AMD Sempron™ Processor Ordering Part Number Description

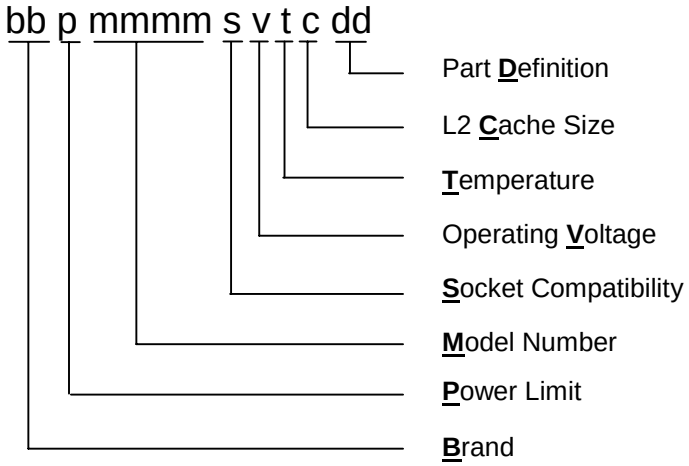


Figure 1. Mobile AMD Sempron™ Processor Ordering Part Number Diagram

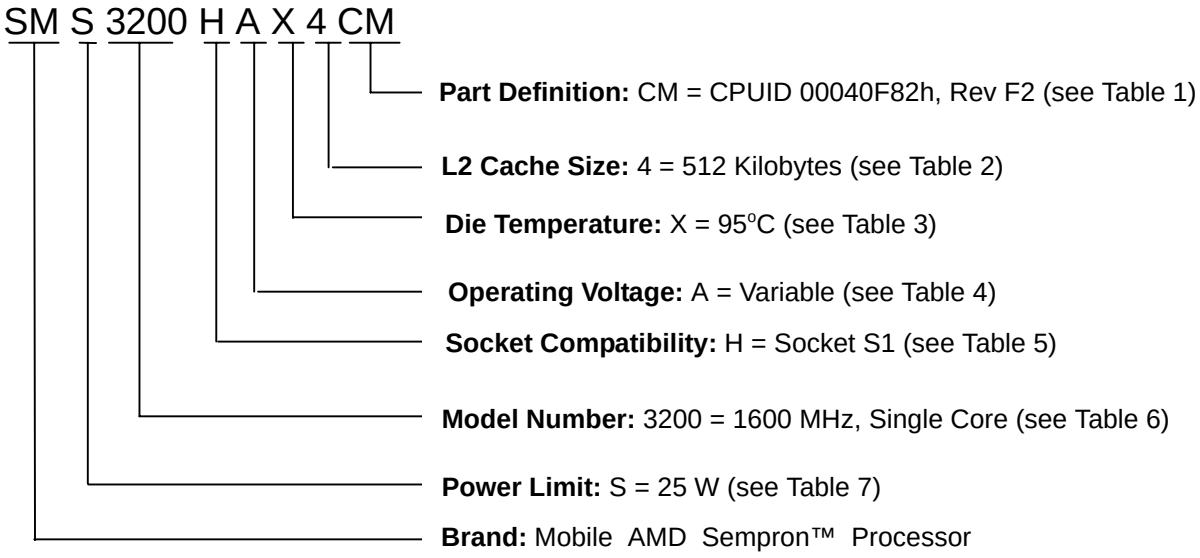


Figure 2. Mobile AMD Sempron™ Processor Ordering Part Number Example

Table 1: Mobile AMD Sempron™ Processor Part Definition Options

Part Definition	Revision	CPUID 8000_0001h EAX [31:0] (CPUID)	Package Drawing
CM	Rev F2	00040FC2h	Lidless H3
DN	Rev G2	00070FC2h	Lidless H4
DQ	Rev G2	00060FC2h	Lidless H5

Table 2: Mobile AMD Sempron™ Processor L2 Cache Size Options

OPN Character	Cache Size
3	256 KB
4	512 KB

Table 3: Mobile AMD Sempron™ Processor Temperature Options

OPN Character	Temperature
X	95°C

Table 4: Mobile AMD Sempron™ Processor Operating Voltage

OPN Character	Operating Voltage
A	Variable

Table 5: Mobile AMD Sempron™ Processor Package Options

OPN Character	Package
H	Socket S1 Processor

Table 6: Mobile AMD Sempron™ Processor Model Number Options

Package	Cache Size	Frequency	Model Number
Socket S1 Processor	256 KB	1000 MHz	2100+
Socket S1 Processor	512 KB	1600 MHz	3200+
Socket S1 Processor	256 KB	1800 MHz	3400+
Socket S1 Processor	512 KB	1800 MHz	3500+
Socket S1 Processor	256 KB	2000 MHz	3600+
Socket S1 Processor	512 KB	2000 MHz	3700+
Socket S1 Processor	256 KB	2200 MHz	3800+
Socket S1 Processor	512 KB	2200 MHz	4000+

Table 7: Mobile AMD Sempron™ Processor Power Limit

OPN Character	Power Limit
D	35 W
S	25 W

2.2 Mobile AMD Sempron™ Processor Thermal and Power Table Guide

The Thermal and Power Table Guide shown in Table 8 maps SOPNs and the properties associated with their defined characters to the proper thermal and power table subsections and page numbers. This table is designed to be used as a quick reference for finding the appropriate subsection for the thermal and power tables corresponding to an SOPN.

Table 8: Mobile AMD Sempron™ Processor Thermal and Power Table Guide

SOPN	Power	Revision	Single/Dual-Core	Thermal/Power Tables
SMD mmmmsvtc **CM**	35 W	Rev F2	Single-Core	Section 2.3.1 on page 18
SMD mmmmsvtc **DN**	35 W	Rev G2	Single-Core	Section 2.3.2 on page 19
SMS mmmmsvtc **CM**	25 W	Rev F2	Single-Core	Section 2.3.3 on page 20
SMS mmmmsvtc **DN**	25 W	Rev G2	Single-Core	Section 2.3.4 on page 22
SMS mmmmsvtc **DQ**	25 W	Rev G2	Single-Core	Section 2.3.5 on page 23

2.3 Mobile AMD Sempron™ Processor Thermal and Power Specifications

The thermal and power specification tables contain the thermal and power requirements for each OPN. This includes the information necessary for thermal management (for example, heat sink requirements, temperature assumptions) and power delivery (for example, voltage, current, and power dissipation for each P-state). For all other electrical specifications for the processor, refer to the *AMD NPT Family 0Fh Processor Electrical Data Sheet*, order #31119. For power management BIOS requirements, refer to the *BIOS and Kernel Developer's Guide for AMD NPT Family 0Fh Processors*, order #32559.

Section 2.1 on page 13 provides an example of the OPN structure for processors documented in this chapter and Table 8 on page 16 provides a guide to OPN organization in the following subsections. Refer to Section 1.2 on page 11 and Section 1.3 on page 12 for numbering conventions and terminology definitions used in these tables.

2.3.1 SMD mmmmsvtc CM 35W, S1, Mobile, Rev F2 Thermal and Power Specifications

Parameter/OPN	Notes	SMD3800HAX3CM		
Tdie Max		95°C		
Tambient		0°C to 35°C		
Trise		10°C		
Thermal Resistance (die-amb)		1.61°C/W		
Max P-State		2200 MHz		
VID_VDD	1	1.225 V	1.275 V	1.300 V
IDD Max		22.86 A		
Thermal Design Power	2,3	31.0 W		
Intermediate P-State #1		2000 MHz		
VID_VDD	1	1.175 V	1.225 V	1.250 V
IDD Max		20.00 A		
Thermal Design Power	2,3	26.5 W		
Intermediate P-State #2		1800 MHz		
VID_VDD	1	1.125 V	1.175 V	1.200 V
IDD Max		17.24 A		
Thermal Design Power	2,3	22.4 W		
Intermediate P-State #3		1600 MHz		
VID_VDD	1	1.075 V	1.125 V	1.150 V
IDD Max		14.79 A		
Thermal Design Power	2,3	18.9 W		
Intermediate P-State #4		N/A		
VID_VDD	1			
IDD Max				
Thermal Design Power	2,3			
Intermediate P-State #5		N/A		
VID_VDD	1			
IDD Max				
Thermal Design Power	2,3			
Intermediate P-State #6		N/A		
VID_VDD	1			
IDD Max				
Thermal Design Power	2,3			
Min P-State		800 MHz		
VID_VDD	1	0.950 V		
IDD Max		11.58 A		
Thermal Design Power	2,3	14.0 W		
Halt/Stop Grant				
IDDC1 Max @ Max P-State	4	6.82 A		
IDDC1 Max @ Min P-State	5	2.50 A		
I/O Power	7,8	3.0 W		
C3/S1 Min P-State VID_VDD	9			
IDDC3 Max	10	2.40 A		
I/O Power	7,8	1.2 W		
S3	10			
I/O Power	7,8,11	250 mW		

The notes for this table are on page 24.

2.3.2 SMD mmmmsvtc DN 35W, S1, Mobile, Rev G2 Thermal and Power Specifications

Parameter/OPN	Notes	SMD3800HAX3DN			SMD4000HAX4DN		
Tdie Max		95°C			95°C		
Tambient		0°C to 35°C			0°C to 35°C		
Trise		10°C			10°C		
Thermal Resistance (die-amb)		1.61°C/W			1.61°C/W		
Max P-State		2200 MHz			2200 MHz		
VID_VDD	1	1.150 V	1.200 V	1.250 V	1.150 V	1.200 V	1.250 V
IDD Max		24.35 A			24.35 A		
Thermal Design Power	2,3	31.0 W			31.0 W		
Intermediate P-State #1		2000 MHz			2000 MHz		
VID_VDD	1	1.125 V	1.175 V	1.225 V	1.125 V	1.175 V	1.225 V
IDD Max		21.96 A			21.96 A		
Thermal Design Power	2,3	27.7 W			27.7 W		
Intermediate P-State #2		1800 MHz			1800 MHz		
VID_VDD	1	1.100 V	1.150 V	1.200 V	1.100 V	1.150 V	1.200 V
IDD Max		19.64 A			19.64 A		
Thermal Design Power	2,3	24.6 W			24.6 W		
Intermediate P-State #3		1600 MHz			1600 MHz		
VID_VDD	1	1.075 V	1.100 V	1.150 V	1.075 V	1.100 V	1.150 V
IDD Max		17.49 A			17.49 A		
Thermal Design Power	2,3	21.8 W			21.8 W		
Intermediate P-State #4		N/A			N/A		
VID_VDD	1						
IDD Max							
Thermal Design Power	2,3						
Intermediate P-State #5		N/A			N/A		
VID_VDD	1						
IDD Max							
Thermal Design Power	2,3						
Intermediate P-State #6		N/A			N/A		
VID_VDD	1						
IDD Max							
Thermal Design Power	2,3						
Min P-State		800 MHz			800 MHz		
VID_VDD	1	0.950 V			0.950 V		
IDD Max		11.58 A			11.58 A		
Thermal Design Power	2,3	14.0 W			14.0 W		
Halt/Stop Grant							
IDDC1 Max @ Max P-State	4	6.82 A			6.82 A		
IDDC1 Max @ Min P-State	5	2.50 A			2.50 A		
I/O Power	7,8	3.0 W			3.0 W		
C3/S1 Min P-State VID_VDD	9						
IDDC3 Max	10	2.40 A			2.40 A		
I/O Power	7,8	1.2 W			1.2 W		
S3	10						
I/O Power	7,8,11	250 mW			250 mW		

The notes for this table are on page 24.

2.3.3 SMS mmmmsvtc CM 25W, S1, Mobile, Rev F2 Thermal and Power Specifications

Parameter/OPN	Notes	SMS3200HAX4CM			SMS3400HAX3CM			SMS3500HAX4CM		
Tdie Max		95°C			95°C			95°C		
Tambient		0°C to 35°C			0°C to 35°C			0°C to 35°C		
Trise		10°C			10°C			10°C		
Thermal Resistance (die-amb)		2.00°C/W			2.00°C/W			2.00°C/W		
Max P-State		1600 MHz			1800 MHz			1800 MHz		
VID_VDD	1	1.125 V	1.150 V	1.200 V	1.125 V	1.150 V	1.200 V	1.125 V	1.150 V	1.200 V
IDD Max		19.6 A			19.6 A			19.6 A		
Thermal Design Power	2,3	25.0 W			25.0 W			25.0 W		
Intermediate P-State #1		N/A			1600 MHz			1600 MHz		
VID_VDD	1				1.075 V	1.100 V	1.150 V	1.075 V	1.100 V	1.150 V
IDD Max					16.4 A			16.4 A		
Thermal Design Power	2,3				20.6 W			20.6 W		
Intermediate P-State #2		N/A			N/A			N/A		
VID_VDD	1									
IDD Max										
Thermal Design Power	2,3									
Intermediate P-State #3		N/A			N/A			N/A		
VID_VDD	1									
IDD Max										
Thermal Design Power	2,3									
Intermediate P-State #4		N/A			N/A			N/A		
VID_VDD	1									
IDD Max										
Thermal Design Power	2,3									
Intermediate P-State #5		N/A			N/A			N/A		
VID_VDD	1									
IDD Max										
Thermal Design Power	2,3									
Intermediate P-State #6		N/A			N/A			N/A		
VID_VDD	1									
IDD Max										
Thermal Design Power	2,3									
Min P-State		800 MHz			800 MHz			800 MHz		
VID_VDD	1	0.950 V			0.950 V			0.950 V		
IDD Max		8.4 A			8.4 A			8.4 A		
Thermal Design Power	2,3	11.0 W			11.0 W			11.0 W		
Halt/Stop Grant										
IDDC1 Max @ Max P-State	4	9.3 A			8.0 A			8.0 A		
IDDC1 Max @ Min P-State	5	2.5 A			2.5 A			2.5 A		
I/O Power	7,8	3.0 W			3.0 W			3.0 W		
C3/S1 Min P-State VID_VDD	9									
IDDC3 Max	10	2.4 A			2.4 A			2.4 A		
I/O Power	7,8	1.2 W			1.2 W			1.2 W		
C3/S1 AltVID		N/A			N/A			N/A		
VID_VDD		N/A			N/A			N/A		
IDDC3 Max										
I/O Power										
S3	10									
I/O Power	7,8,11	250 mW			250 mW			250 mW		

The notes for this table are on page 24.

Parameter/OPN	Notes	SMS3600HAX3CM		
Tdie Max		95°C		
Tambient		0°C to 35°C		
Trise		10°C		
Thermal Resistance (die-amb)		2.00°C/W		
Max P-State		2000 MHz		
VID_VDD	1	1.125 V	1.150 V	1.200 V
IDD Max		19.6 A		
Thermal Design Power	2,3	25.0 W		
Intermediate P-State #1		1800 MHz		
VID_VDD	1	1.075 V	1.100 V	1.150 V
IDD Max		16.6 A		
Thermal Design Power	2,3	20.8 W		
Intermediate P-State #2		1600 MHz		
VID_VDD	1	1.025 V	1.050 V	1.100 V
IDD Max		13.9 A		
Thermal Design Power	2,3	17.2 W		
Intermediate P-State #3		N/A		
VID_VDD	1			
IDD Max				
Thermal Design Power	2,3			
Intermediate P-State #4		N/A		
VID_VDD	1			
IDD Max				
Thermal Design Power	2,3			
Intermediate P-State #5		N/A		
VID_VDD	1			
IDD Max				
Thermal Design Power	2,3			
Intermediate P-State #6		N/A		
VID_VDD	1			
IDD Max				
Thermal Design Power	2,3			
Min P-State		800 MHz		
VID_VDD	1	0.950 V		
IDD Max		8.4 A		
Thermal Design Power	2,3	11.0 W		
Halt/Stop Grant				
IDDC1 Max @ Max P-State	4	6.7 A		
IDDC1 Max @ Min P-State	5	2.5 A		
I/O Power	7,8	3.0 W		
C3/S1 Min P-State VID_VDD	9			
IDDC3 Max	10	2.4 A		
I/O Power	7,8	1.2 W		
C3/S1 AltVID		N/A		
VID_VDD		N/A		
IDDC3 Max				
I/O Power				
S3	10			
I/O Power	7,8,11	250 mW		

The notes for this table are on page 24.

2.3.4 SMS mmmmsvtc DN 25W, S1, Mobile, Rev G2 Thermal and Power Specifications

Parameter/OPN	Notes	SMS3600HAX3DN		
Tdie Max		95°C		
Tambient		0°C to 35°C		
Trise		10°C		
Thermal Resistance (die-amb)		2.00°C/W		
Max P-State		2000 MHz		
VID_VDD	1	1.150 V	1.200 V	1.250 V
IDD Max		19.1 A		
Thermal Design Power	2,3	25.0 W		
Intermediate P-State #1		1800 MHz		
VID_VDD	1	1.125 V	1.175 V	1.225 V
IDD Max		17.1 A		
Thermal Design Power	2,3	22.2 W		
Intermediate P-State #2		1600 MHz		
VID_VDD	1	1.100 V	1.150 V	1.200 V
IDD Max		15.2 A		
Thermal Design Power	2,3	19.7 W		
Intermediate P-State #3		N/A		
VID_VDD	1			
IDD Max				
Thermal Design Power	2,3			
Intermediate P-State #4		N/A		
VID_VDD	1			
IDD Max				
Thermal Design Power	2,3			
Intermediate P-State #5		N/A		
VID_VDD	1			
IDD Max				
Thermal Design Power	2,3			
Intermediate P-State #6		N/A		
VID_VDD	1			
IDD Max				
Thermal Design Power	2,3			
Min P-State		800 MHz		
VID_VDD	1	0.950 V		
IDD Max		11.6 A		
Thermal Design Power	2,3	14.0 W		
Halt/Stop Grant				
IDDC1 Max @ Max P-State	4	10.2 A		
IDDC1 Max @ Min P-State	5	2.5 A		
I/O Power	7,8	3.0 W		
C3/S1 Min P-State VID_VDD	9			
IDDC3 Max	10	2.4 A		
I/O Power	7,8	1.2 W		
C3/S1 AltVID		N/A		
VID_VDD		N/A		
IDDC3 Max				
I/O Power				
S3	10			
I/O Power	7,8,11	250 mW		

The notes for this table are on page 24.

2.3.5 SMS mmmmsvtc DQ 25W, S1, Embedded Mobile, Rev G2 Thermal and Power Specifications

Parameter/OPN	Notes	SMS3700HAX4DQ		
Tdie Max		95°C		
Minimum Tambient		0°C		
Max P-State		2000 MHz		
VID_VDD	1	1.150 V	1.200 V	1.250 V
IDD Max		19.1 A		
Thermal Design Power	2,3	25.0 W		
Intermediate P-State #1		1800 MHz		
VID_VDD	1	1.125 V	1.175 V	1.225 V
IDD Max		17.1 A		
Thermal Design Power	2,3	22.2 W		
Intermediate P-State #2		1600 MHz		
VID_VDD	1	1.100 V	1.150 V	1.200 V
IDD Max		15.2 A		
Thermal Design Power	2,3	19.7 W		
Intermediate P-State #3		N/A		
VID_VDD	1			
IDD Max				
Thermal Design Power	2,3			
Intermediate P-State #4		N/A		
VID_VDD	1			
IDD Max				
Thermal Design Power	2,3			
Intermediate P-State #5		N/A		
VID_VDD	1			
IDD Max				
Thermal Design Power	2,3			
Intermediate P-State #6		N/A		
VID_VDD	1			
IDD Max				
Thermal Design Power	2,3			
Min P-State		800 MHz		
VID_VDD	1	0.950 V		
IDD Max		11.6 A		
Thermal Design Power	2,3	14.0 W		
Halt/Stop Grant				
IDDC1 Max @ Max P-State	4	10.2 A		
IDDC1 Max @ Min P-State	5	2.5 A		
I/O Power	7,8	3.0 W		
C3/S1 Min P-State VID_VDD	9			
IDDC3 Max	10	2.4 A		
I/O Power	7,8	1.2 W		
C3/S1 AltVID				
VID_VDD		N/A		
IDDC3 Max		N/A		
I/O Power		N/A		
S3	10			
I/O Power	7,8,11	250 mW		

The notes for this table are on page 24.

Mobile AMD Sempron™ Processor Thermal and Power Specification Table Notes:

1. The VID_VDD voltage is the VID[5:0] requested VDD supply level. Refer to the BIOS and Kernel Developer's Guide for AMD NPT Family Processors, order #32559, for details.
2. Thermal Design Power (TDP) is measured under the conditions of Tdie Max, IDD Max, and VDD=VID_VDD, and include all power dissipated on-die from VDD, VDDIO, VLDT, VTT, and VDDA. Contact your Field Application Engineer for more information on TDP specifications.
3. Thermal Design Power (TDP) specifications for dual core processors assume equivalent P-states (Voltage and frequency) and equivalent Tcase conditions for both cores. Refer to the BIOS and Kernel Developer's Guide for AMD NPT Family Processors, order #32559, for details on P-state operation for dual core processors.
4. Assumes Tdie max, max P-state VID_VDD +25 mV, clock divider set to 512.
5. Assumes 50°C, min P-state VID_VDD +50 mV, clock divider set to 512.
6. IDDC1 specifications for dual core processors assume equivalent Voltage, clock divisor, and Tcase conditions for both cores.
7. Thermal Design Power dissipated by the processor VDDIO, VTT, VLDT, and VDDA power planes only.
8. Assumes VDDIO = 1.8 V and VTT = VDDIO / 2.
9. Assumes 35°C, min P-state VID_VDD, clock divider set to 512, HyperTransport™ links disconnected, memory in self-refresh mode, DDR SDRAM interface tri-stated except clocks and CKE pins.
10. Assumes 35°C, VDD, VDDA, and VLDT supplies are off, VDDIO and VTT are powered, memory in self-refresh mode and DDR SDRAM interface tri-stated except CKE pins.
11. Thermal Design Power dissipated by the processor VDDIO and VTT power planes only.

3 AMD Turion™ 64 Mobile Technology

The following sections contain the OPN description and thermal and power specifications for the AMD Turion™ 64 Mobile Technology. Each column in the thermal and power tables represents a specific Ordering Part Number (OPN). Section 3.1 provides an example of the OPN structure for this processor family.

3.1 AMD Turion™ 64 Mobile Technology Ordering Part Number Description

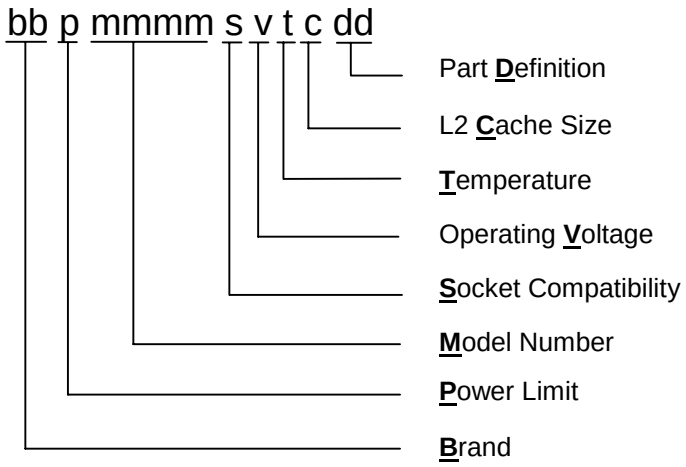


Figure 3. AMD Turion™ 64 Mobile Technology Subsection Ordering Part Number Diagram

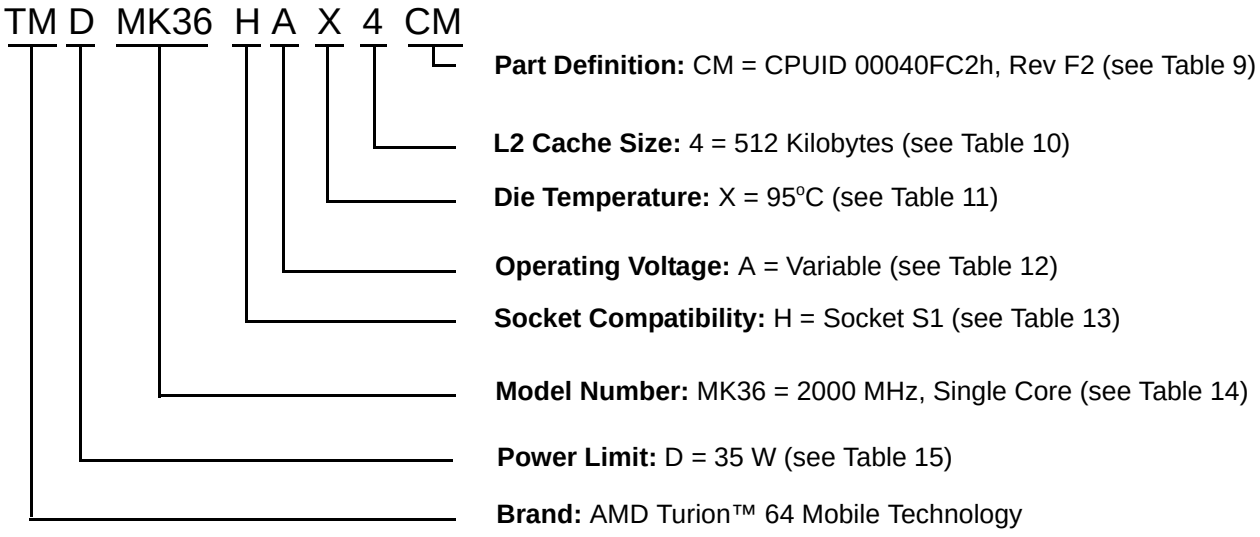


Figure 4. AMD Turion™ 64 Mobile Technology Ordering Part Number Example

Table 9: AMD Turion™ 64 Mobile Technology Part Definition Options

Part Definition	Revision	CPUID 8000_0001h EAX [31:0] (CPUID)	Package Drawing
CM	Rev F2	00040FC2h	Lidless H3

Table 10: AMD Turion™ 64 Mobile Technology L2 Cache Size Options

OPN Character	Cache Size
4	512 KB

Table 11: AMD Turion™ 64 Mobile Technology Temperature Options

OPN Character	Temperature
X	95°C

Table 12: AMD Turion™ 64 Mobile Technology Operating Voltage

OPN Character	Operating Voltage
A	Variable

Table 13: AMD Turion™ 64 Mobile Technology Package Options

OPN Character	Package
H	Socket S1 Processor

Table 14: AMD Turion™ 64 Mobile Technology Model Number Options

Package	Cache Size	Frequency	Model Number
Socket S1 Processor	512 KB	2000 MHz	MK36
Socket S1 Processor	512 KB	2200 MHz	MK38

Table 15: AMD Turion™ 64 Mobile Technology Power Limit

OPN Character	Power Limit
D	35 W

3.2 AMD Turion™ 64 Mobile Technology Thermal and Power Table Guide

The thermal and power table guide shown in Table 16 maps SOPNs and the properties associated with their defined characters to the proper Thermal and Power Table subsections and page numbers. This table is designed to be used as a quick reference for finding the appropriate subsection for the thermal and power tables corresponding to an SOPN.

Table 16: AMD Turion™ 64 Mobile Technology Thermal and Power Table Guide

SOPN	Power	Revision	Single/Dual-Core	Thermal/Power Tables
TMD mmmmsvtc **CM**	35 W	Rev F2	Single-Core	Section 3.3.1 on page 29

3.3 AMD Turion™ 64 Mobile Technology Thermal and Power Specifications

The thermal and power specification tables contain the thermal and power requirements for each OPN. This includes the information necessary for thermal management (for example, heat sink requirements, temperature assumptions) and power delivery (for example, voltage, current, and power dissipation for each P-state). For all other electrical specifications for the processor, refer to the *AMD NPT Family 0Fh Processor Electrical Data Sheet*, order #31119. For power management BIOS requirements, refer to the *BIOS and Kernel Developer's Guide for AMD NPT Family 0Fh Processors*, order #32559.

Section 3.1 on page 25 provides an example of the OPN structure for processors documented in this chapter and Table 16 on page 27 provides a guide to OPN organization in the following subsections. Refer to Section 1.2 on page 11 and Section 1.3 on page 12 for numbering conventions and terminology definitions used in these tables.

3.3.1 **TMD** mmmmsvtc **CM 35W, S1, Mobile, Rev F2 Thermal and Power Specifications**

Parameter/OPN	**Notes**	**TMDMK36HAX4CM**			**TMDMK38HAX4CM**		
Tdie Max		95°C			95°C		
Tambient		0°C to 35°C			0°C to 35°C		
Trise		10°C			10°C		
Thermal Resistance (die-amb)		1.63°C/W			1.61°C/W		
Max P-State		2000 MHz			2200 MHz		
VID_VDD	1	1.125 V	1.150 V	1.200 V	1.225 V	1.275 V	1.300 V
IDD Max		24.62 A			22.86 A		
Thermal Design Power	2,3	30.7 W			31.0 W		
Intermediate P-State #1		1800 MHz			2000 MHz		
VID_VDD	1	1.075 V	1.100 V	1.150 V	1.175 V	1.225 V	1.250 V
IDD Max		20.84 A			20.00 A		
Thermal Design Power	2,3	25.4 W			26.5 W		
Intermediate P-State #2		1600 MHz			1800 MHz		
VID_VDD	1	1.025 V	1.050 V	1.100 V	1.125 V	1.175 V	1.200 V
IDD Max		17.46 A			17.24 A		
Thermal Design Power	2,3	20.9 W			22.4 W		
Intermediate P-State #3		N/A			1600 MHz		
VID_VDD	1				1.075 V	1.125 V	1.150 V
IDD Max					14.79 A		
Thermal Design Power	2,3				18.9 W		
Intermediate P-State #4		N/A			N/A		
VID_VDD	1						
IDD Max							
Thermal Design Power	2,3						
Intermediate P-State #5		N/A			N/A		
VID_VDD	1						
IDD Max							
Thermal Design Power	2,3						
Intermediate P-State #6		N/A			N/A		
VID_VDD	1						
IDD Max							
Thermal Design Power	2,3						
Min P-State		800 MHz			800 MHz		
VID_VDD	1	0.950 V			0.950 V		
IDD Max		9.47 A			8.42 A		
Thermal Design Power	2,3	12.0 W			11.0 W		
Halt/Stop Grant							
IDDC1 Max @ Max P-State	4	6.80 A			6.80 A		
IDDC1 Max @ Min P-State	5	1.80 A			1.80 A		
I/O Power	7,8	3.0 W			3.0 W		
C3/S1 Min P-State VID_VDD	9						
IDDC3 Max		1.37 A			1.37 A		
I/O Power	7,8	350 mW			350 mW		
S3	10						
I/O Power	7,8,11	250 mW			250 mW		

The notes for this table are on page 30.

AMD Turion™ 64 Mobile Technology Thermal and Power Specification Table Notes:

1. The VID_VDD voltage is the VID[5:0] requested VDD supply level. Refer to the BIOS and Kernel Developer's Guide for AMD NPT Family Processors, order #32559, for details.
2. Thermal Design Power (TDP) is measured under the conditions of Tdie Max, IDD Max, and VDD=VID_VDD, and include all power dissipated on-die from VDD, VDDIO, VLDT, VTT, and VDDA. Contact your Field Application Engineer for more information on TDP specifications.
3. Thermal Design Power (TDP) specifications for dual core processors assume equivalent P-states (Voltage and frequency) and equivalent Tcase conditions for both cores. Refer to the BIOS and Kernel Developer's Guide for AMD NPT Family Processors, order #32559, for details on P-state operation for dual core processors.
4. Assumes Tdie max, max P-state VID_VDD +25 mV, clock divider set to 512.
5. Assumes 50°C, min P-state VID_VDD +50 mV, clock divider set to 512.
6. IDDC1 specifications for dual core processors assume equivalent Voltage, clock divisor, and Tcase conditions for both cores.
7. Thermal Design Power dissipated by the processor VDDIO, VTT, VLDT, and VDDA power planes only.
8. Assumes VDDIO = 1.8 V and VTT = VDDIO / 2.
9. Assumes 35°C, min P-state VID_VDD, clock divider set to 512, HyperTransport™ links disconnected, memory in self-refresh mode, DDR SDRAM interface tri-stated except CKE pins.
10. Assumes 35°C, VDD, VDDA, and VLDT supplies are off, VDDIO and VTT are powered, memory in self-refresh mode and DDR SDRAM interface tri-stated except CKE pins.
11. Thermal Design Power dissipated by the processor VDDIO and VTT power planes only.

4 AMD Turion™ 64 X2 Mobile Technology

The following sections contain the OPN description and thermal and power specifications for the AMD Turion™ 64 X2 Mobile Technology. Each column in the thermal and power tables represents a specific Ordering Part Number (OPN). Section 4.1 provides an example of the OPN structure for this processor family.

4.1 AMD Turion™ 64 X2 Mobile Technology Ordering Part Number Description

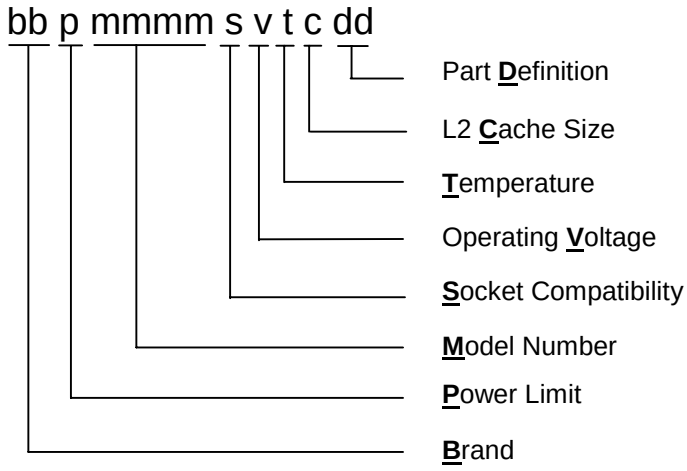


Figure 5. AMD Turion™ 64 X2 Mobile Technology Subsection Ordering Part Number Diagram

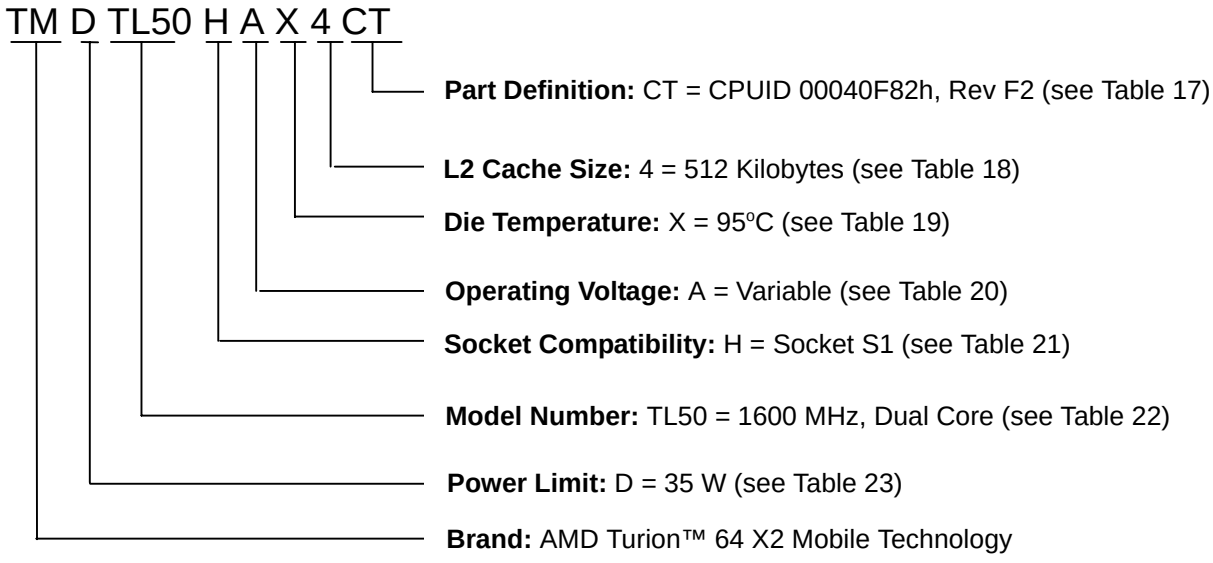


Figure 6. AMD Turion™ 64 X2 Mobile Technology Ordering Part Number Example

Table 17: AMD Turion™ 64 X2 Mobile Technology Part Definition Options

Part Definition	Revision	CPUID 8000_0001h EAX [31:0] (CPUID)	Package Drawing
CT	Rev F2	00040F82h	Lidless H2
DC	Rev G1	00060F81h	Lidless H4
DM	Rev G2	00060F82h	Lidless H4

Table 18: AMD Turion™ 64 X2 Mobile Technology L2 Cache Size Options

OPN Character	Cache Size
4	512 KB
5	1 MB

Table 19: AMD Turion™ 64 X2 Mobile Technology Temperature Options

OPN Character	Temperature
X	95°C

Table 20: AMD Turion™ 64 X2 Mobile Technology Operating Voltage

OPN Character	Operating Voltage
A	Variable

Table 21: AMD Turion™ 64 X2 Mobile Technology Package Options

OPN Character	Package
H	Socket S1 Processor

Table 22: AMD Turion™ 64 X2 Mobile Technology Model Number Options

Package	Cache Size	Frequency	Model Number
Socket S1 Processor	512 KB	1600 MHz	TL50
Socket S1 Processor	1 MB	1600 MHz	TL52
Socket S1 Processor	1 MB	1800 MHz	TL56
Socket S1 Processor	1 MB	1900 MHz	TL58
Socket S1 Processor	1 MB	2000 MHz	TL60
Socket S1 Processor	1 MB	2100 MHz	TL62
Socket S1 Processor	1 MB	2200 MHz	TL64
Socket S1 Processor	1 MB	2300 MHz	TL66
Socket S1 Processor	1 MB	2400 MHz	TL68

Table 23: AMD Turion™ 64 X2 Mobile Technology Power Limit

OPN Character	Power Limit
D	35 W

4.2 AMD Turion™ 64 X2 Mobile Technology Thermal and Power Table Guide

The thermal and power table guide shown in Table 24 maps SOPNs and the properties associated with their defined characters to the proper Thermal and Power Table subsections and page numbers. This table is designed to be used as a quick reference for finding the appropriate subsection for the thermal and power tables corresponding to an SOPN.

Table 24: AMD Turion™ 64 X2 Mobile Technology Thermal and Power Table Guide

SOPN	Power	Revision	Single/Dual-Core	Thermal/Power Tables
TMD mmmmsvtc **CT**	35 W	Rev F2	Dual-Core	Section 4.3.1 on page 36
TMD mmmmsvtc **DC**	35 W	Rev G1	Dual-Core	Section 4.3.2 on page 38
TMD mmmmsvtc **DM**	35 W	Rev G2	Dual-Core	Section 4.3.3 on page 40

4.3 AMD Turion™ 64 X2 Mobile Technology Thermal and Power Specifications

The thermal and power specification tables contain the thermal and power requirements for each OPN. This includes the information necessary for thermal management (for example, heat sink requirements, temperature assumptions) and power delivery (for example, voltage, current, and power dissipation for each P-state). For all other electrical specifications for the processor, refer to the *AMD NPT Family 0Fh Processor Electrical Data Sheet*, order #31119. For power management BIOS requirements, refer to the *BIOS and Kernel Developer's Guide for AMD NPT Family 0Fh Processors*, order #32559.

Section 4.1 on page 31 provides an example of the OPN structure for processors documented in this chapter and Table 24 on page 34 provides a guide to OPN organization in the following subsections. Refer to Section 1.2 on page 11 and Section 1.3 on page 12 for numbering conventions and terminology definitions used in these tables.

4.3.1 **TMD** mmmmsvtc **CT 35W, S1, Mobile, Rev F2 Thermal and Power Specifications**

Parameter/OPN	**Notes**	**TMDTL50HAX4CT**	**TMDTL52HAX5CT**	**TMDTL56HAX5CT**
Tdie Max		95°C	95°C	95°C
Tambient		0°C to 35°C	0°C to 35°C	0°C to 35°C
Trise		10°C	10°C	10°C
Thermal Resistance (die-amb)		1.61°C/W	1.61°C/W	1.52°C/W
Max P-State		1600 MHz	1600 MHz	1800 MHz
VID_VDD	1	1.075 V / 1.100 V	1.075 V / 1.100 V	1.075 V / 1.100 V
IDD Max		26.05 A	26.05 A	27.91 A
Thermal Design Power	2,3	31.0 W	31.0 W	33.0 W
Intermediate P-State #1		N/A	N/A	1600 MHz
VID_VDD	1			1.025 V / 1.050 V
IDD Max				25.85 A
Thermal Design Power	2,3			29.5 W
Intermediate P-State #2		N/A	N/A	N/A
VID_VDD	1			
IDD Max				
Thermal Design Power	2,3			
Intermediate P-State #3		N/A	N/A	N/A
VID_VDD	1			
IDD Max				
Thermal Design Power	2,3			
Intermediate P-State #4		N/A	N/A	N/A
VID_VDD	1			
IDD Max				
Thermal Design Power	2,3			
Intermediate P-State #5		N/A	N/A	N/A
VID_VDD	1			
IDD Max				
Thermal Design Power	2,3			
Intermediate P-State #6		N/A	N/A	N/A
VID_VDD	1			
IDD Max				
Thermal Design Power	2,3			
Min P-State		800 MHz	800 MHz	800 MHz
VID_VDD	1	0.800 V	0.800 V	0.800 V
IDD Max		10.00 A	10.00 A	10.00 A
Thermal Design Power	2,3	11.0 W	11.0 W	11.0 W
Halt/Stop Grant				
IDDC1 Max @ Max P-State	4	6.81 A	6.81 A	6.22 A
IDDC1 Max @ Min P-State	5	1.88 A	1.88 A	1.88 A
I/O Power	7,8	3.0 W	3.0 W	3.0 W
C1E/S1 Min P-State VID_VDD	9			
IDDC1E Max		0.88 A	0.88 A	0.88 A
I/O Power	7,8	350 mW	350 mW	350 mW
C1E/S1 AltVID	12			
VID_VDD	13	0.750 V	0.750 V	0.750 V
IDDC1E Max		0.67 A	0.67 A	0.67 A
I/O Power	7,8	350 mW	350 mW	350 mW
S3	10			
I/O Power	7,8,11	250 mW	250 mW	250 mW

The notes for this table are on page 43.

Parameter/OPN	Notes	TMDTL60HAX5CT		TMDTL64HAX5CT	
Tdie Max		95°C		95°C	
Tambient		0°C to 35°C		0°C to 35°C	
Trise		10°C		10°C	
Thermal Resistance (die-amb)		1.43°C/W		1.43°C/W	
Max P-State		2000 MHz		2200 MHz	
VID_VDD	1	1.075 V	1.100 V	1.075 V	1.100 V
IDD Max		29.77 A		29.77 A	
Thermal Design Power	2,3	35.0 W		35.0 W	
Intermediate P-State #1		1800 MHz		2000 MHz	
VID_VDD	1	1.025 V	1.050 V	1.025 V	1.050 V
IDD Max		26.05 A		25.46 A	
Thermal Design Power	2,3	29.7 W		29.1 W	
Intermediate P-State #2		1600 MHz		1800 MHz	
VID_VDD	1	0.975 V	1.000 V	0.975 V	1.000 V
IDD Max		20.82 A		21.64 A	
Thermal Design Power	2,3	23.3 W		24.1 W	
Intermediate P-State #3		N/A		1600 MHz	
VID_VDD	1			0.925 V	0.950 V
IDD Max				18.38 A	
Thermal Design Power	2,3			20.0 W	
Intermediate P-State #4		N/A		N/A	
VID_VDD	1				
IDD Max					
Thermal Design Power	2,3				
Intermediate P-State #5		N/A		N/A	
VID_VDD	1				
IDD Max					
Thermal Design Power	2,3				
Intermediate P-State #6		N/A		N/A	
VID_VDD	1				
IDD Max					
Thermal Design Power	2,3				
Min P-State		800 MHz		800 MHz	
VID_VDD	1	0.800 V		0.800 V	
IDD Max		10.00 A		10.00 A	
Thermal Design Power	2,3	11.0 W		11.0 W	
Halt/Stop Grant					
IDDC1 Max @ Max P-State	4	5.62 A		3.17 A	
IDDC1 Max @ Min P-State	5	1.88 A		1.88 A	
I/O Power	7,8	3.0 W		3.0 W	
C1E/S1 Min P-State VID_VDD	9				
IDDC1E Max		0.88 A		0.88 A	
I/O Power	7,8	350 mW		350 mW	
C1E/S1 AltVID	12				
VID_VDD	13	0.750 V		0.750 V	
IDDC1E Max		0.67 A		0.67 A	
I/O Power	7,8	350 mW		350 mW	
S3	10				
I/O Power	7,8,11	250 mW		250 mW	

The notes for this table are on page 43.

4.3.2 **TMD** mmmmsvtc **DC 35W, S1, Mobile, Rev G1 Thermal and Power Specifications**

Parameter/OPN	**Notes**	**TMDTL56HAX5DC**	**TMDTL58HAX5DC**	**TMDTL60HAX5DC**
Tdie Max		95°C	95°C	95°C
Tambient		0°C to 35°C	0°C to 35°C	0°C to 35°C
Trise		10°C	10°C	10°C
Thermal Resistance (die-amb)		1.61°C/W	1.61°C/W	1.61°C/W
Max P-State		1800 MHz	1900 MHz	2000 MHz
VID_VDD	1	1.075 V | 1.100 V | 1.125 V	1.075 V | 1.100 V | 1.125 V	1.075 V | 1.100 V | 1.125 V
IDD Max		26.05 A	26.05 A	26.05 A
Thermal Design Power	2,3	31.0 W	31.0 W	31.0 W
Intermediate P-State #1		1600 MHz	1800 MHz	1800 MHz
VID_VDD	1	1.050 V | 1.075 V | 1.100 V	1.050 V | 1.075 V | 1.100 V	1.050 V | 1.075 V | 1.100 V
IDD Max		22.95 A	23.90 A	23.05 A
Thermal Design Power	2,3	27.1 W	28.1 W	27.2 W
Intermediate P-State #2		N/A	1600 MHz	1600 MHz
VID_VDD	1		1.025 V | 1.050 V | 1.075 V	1.025 V | 1.050 V | 1.075 V
IDD Max			20.98 A	20.20 A
Thermal Design Power	2,3		24.5 W	23.7 W
Intermediate P-State #3		N/A	N/A	N/A
VID_VDD	1			
IDD Max				
Thermal Design Power	2,3			
Intermediate P-State #4		N/A	N/A	N/A
VID_VDD	1			
IDD Max				
Thermal Design Power	2,3			
Intermediate P-State #5		N/A	N/A	N/A
VID_VDD	1			
IDD Max				
Thermal Design Power	2,3			
Intermediate P-State #6		N/A	N/A	N/A
VID_VDD	1			
IDD Max				
Thermal Design Power	2,3			
Min P-State		800 MHz	800 MHz	800 MHz
VID_VDD	1	0.800 V	0.800 V	0.800 V
IDD Max		8.00 A	8.00 A	8.00 A
Thermal Design Power	2,3	9.4 W	9.4 W	9.4 W
Halt/Stop Grant				
IDDC1 Max @ Max P-State	4	6.70 A	6.35 A	6.20 A
IDDC1 Max @ Min P-State	5	1.50 A	1.50 A	1.50 A
I/O Power	7,8	3.0 W	3.0 W	3.0 W
C1E/S1 Min P-State VID_VDD	9			
IDDC1E Max		0.88 A	0.88 A	0.88 A
I/O Power	7,8	350 mW	350 mW	350 mW
C1E/S1 AltVID	12			
VID_VDD	13	0.750 V	0.750 V	0.750 V
IDDC1E Max		0.67 A	0.67 A	0.67 A
I/O Power	7,8	350 mW	350 mW	350 mW
S3	10			
I/O Power	7,8,11	200 mW	200 mW	200 mW

The notes for this table are on page 43.

Parameter/OPN	Notes	TMDTL64HAX5DC			TMDTL66HAX5DC		
Tdie Max		95°C			95°C		
Tambient		0°C to 35°C			0°C to 35°C		
Trise		10°C			10°C		
Thermal Resistance (die-amb)		1.43°C/W			1.43°C/W		
Max P-State		2200 MHz			2300 MHz		
VID_VDD	1	1.100 V	1.125 V	1.150 V	1.100 V	1.125 V	1.150 V
IDD Max		29.09 A			29.09 A		
Thermal Design Power	2,3	35.0 W			35.0 W		
Intermediate P-State #1		2000 MHz			2200 MHz		
VID_VDD	1	1.075 V	1.100 V	1.125 V	1.075 V	1.100 V	1.125 V
IDD Max		25.86 A			26.98 A		
Thermal Design Power	2,3	30.8 W			32.0 W		
Intermediate P-State #2		1800 MHz			2000 MHz		
VID_VDD	1	1.050 V	1.075 V	1.100 V	1.050 V	1.075 V	1.100 V
IDD Max		22.86 A			23.90 A		
Thermal Design Power	2,3	27.0 W			28.1 W		
Intermediate P-State #3		1600 MHz			1800 MHz		
VID_VDD	1	1.025 V	1.050 V	1.075 V	1.025 V	1.050 V	1.075 V
IDD Max		20.10 A			21.07 A		
Thermal Design Power	2,3	23.6 W			24.6 W		
Intermediate P-State #4		N/A			1600 MHz		
VID_VDD	1				1.000 V	1.025 V	1.050 V
IDD Max					18.40 A		
Thermal Design Power	2,3				21.4 W		
Intermediate P-State #5		N/A			N/A		
VID_VDD	1						
IDD Max							
Thermal Design Power	2,3						
Intermediate P-State #6		N/A			N/A		
VID_VDD	1						
IDD Max							
Thermal Design Power	2,3						
Min P-State		800 MHz			800 MHz		
VID_VDD	1	0.800 V			0.800 V		
IDD Max		8.00 A			8.00 A		
Thermal Design Power	2,3	9.4 W			9.4 W		
Halt/Stop Grant							
IDDC1 Max @ Max P-State	4	7.36 A			7.35 A		
IDDC1 Max @ Min P-State	5	1.50 A			1.50 A		
I/O Power	7,8	3.0 W			3.0 W		
C1E/S1 Min P-State VID_VDD	9						
IDDC1E Max		0.88 A			0.88 A		
I/O Power	7,8	350 mW			350 mW		
C1E/S1 AltVID	12						
VID_VDD	13,	0.750 V			0.750 V		
IDDC1E Max		0.67 A			0.67 A		
I/O Power	7,8	350 mW			350 mW		
S3	10						
I/O Power	7,8,11	200 mW			200 mW		

The notes for this table are on page 43.

4.3.3 **TMD** mmmmsvtc **DM 35W, S1, Mobile, Rev G2 Thermal and Power Specifications**

Parameter/OPN	Notes	TMDTL56HAX5DM			TMDTL58HAX5DM			TMDTL60HAX5DM		
Tdie Max		95°C			95°C			95°C		
Tambient		0°C to 35°C			0°C to 35°C			0°C to 35°C		
Trise		10°C			10°C			10°C		
Thermal Resistance (die-amb)		1.61°C/W			1.61°C/W			1.61°C/W		
Max P-State		1800 MHz			1900 MHz			2000 MHz		
VID_VDD	1	1.075 V	1.100 V	1.125 V	1.075 V	1.100 V	1.125 V	1.075 V	1.100 V	1.125 V
IDD Max		26.05 A			26.05 A			26.05 A		
Thermal Design Power	2,3	31.0 W			31.0 W			31.0 W		
Intermediate P-State #1		1600 MHz			1800 MHz			1800 MHz		
VID_VDD	1	1.050 V	1.075 V	1.100 V	1.050 V	1.075 V	1.100 V	1.050 V	1.075 V	1.100 V
IDD Max		22.95 A			23.90 A			23.05 A		
Thermal Design Power	2,3	27.1 W			28.1 W			27.2 W		
Intermediate P-State #2		N/A			1600 MHz			1600 MHz		
VID_VDD	1				1.025 V	1.050 V	1.075 V	1.025 V	1.050 V	1.075 V
IDD Max					20.98 A			20.20 A		
Thermal Design Power	2,3				24.5 W			23.7 W		
Intermediate P-State #3		N/A			N/A			N/A		
VID_VDD	1									
IDD Max										
Thermal Design Power	2,3									
Intermediate P-State #4		N/A			N/A			N/A		
VID_VDD	1									
IDD Max										
Thermal Design Power	2,3									
Intermediate P-State #5		N/A			N/A			N/A		
VID_VDD	1									
IDD Max										
Thermal Design Power	2,3									
Intermediate P-State #6		N/A			N/A			N/A		
VID_VDD	1									
IDD Max										
Thermal Design Power	2,3									
Min P-State		800 MHz			800 MHz			800 MHz		
VID_VDD	1	0.800 V			0.800 V			0.800 V		
IDD Max		8.00 A			8.00 A			8.00 A		
Thermal Design Power	2,3	9.4 W			9.4 W			9.4 W		
Halt/Stop Grant										
IDDC1 Max @ Max P-State	4	6.70 A			6.35 A			6.20 A		
IDDC1 Max @ Min P-State	5	1.50 A			1.50 A			1.50 A		
I/O Power	7,8	3.0 W			3.0 W			3.0 W		
C1E/S1 Min P-State VID_VDD	9									
IDDC1E Max		0.88 A			0.88 A			0.88 A		
I/O Power	7,8	350 mW			350 mW			350 mW		
C1E/S1 AltVID	12									
VID_VDD	13	0.750 V			0.750 V			0.750 V		
IDDC1E Max		0.67 A			0.67 A			0.67 A		
I/O Power	7,8	350 mW			350 mW			350 mW		
S3	10									
I/O Power	7,8,11	200 mW			200 mW			200 mW		

The notes for this table are on page 43.

Parameter/OPN	Notes	TMDTL62HAX5DM	TMDTL64HAX5DM	TMDTL66HAX5DM
Tdie Max		95°C	95°C	95°C
Tambient		0°C to 35°C	0°C to 35°C	0°C to 35°C
Trise		10°C	10°C	10°C
Thermal Resistance (die-amb)		1.43°C/W	1.43°C/W	1.43°C/W
Max P-State		2100 MHz	2200 MHz	2300 MHz
VID_VDD	1	1.075 V | 1.100 V | 1.125 V	1.075 V | 1.100 V | 1.125 V	1.075 V | 1.100 V | 1.125 V
IDD Max		29.77 A	29.77 A	29.77 A
Thermal Design Power	2,3	35.0 W	35.0 W	35.0 W
Intermediate P-State #1		2000 MHz	2000 MHz	2200 MHz
VID_VDD	1	1.050 V | 1.075 V | 1.100 V	1.050 V | 1.075 V | 1.100 V	1.050 V | 1.075 V | 1.100 V
IDD Max		25.81 A	26.48 A	27.52 A
Thermal Design Power	2,3	30.1 W	30.8 W	31.9 W
Intermediate P-State #2		1800 MHz	1800 MHz	2000 MHz
VID_VDD	1	1.025 V | 1.050 V | 1.075 V	1.025 V | 1.050 V | 1.075 V	1.025 V | 1.050 V | 1.075 V
IDD Max		22.83 A	23.41 A	24.49 A
Thermal Design Power	2,3	26.4 W	27.0 W	28.1 W
Intermediate P-State #3		1600 MHz	1600 MHz	1800 MHz
VID_VDD	1	1.000 V | 1.025 V | 1.050 V	1.000 V | 1.025 V | 1.050 V	1.000 V | 1.025 V | 1.050 V
IDD Max		20.00 A	20.60 A	21.60 A
Thermal Design Power	2,3	23.0 W	23.6 W	24.6 W
Intermediate P-State #4		N/A	N/A	1600 MHz
VID_VDD	1			0.975 V | 1.000 V | 1.025 V
IDD Max				18.87 A
Thermal Design Power	2,3			21.4 W
Intermediate P-State #5		N/A	N/A	N/A
VID_VDD	1			
IDD Max				
Thermal Design Power	2,3			
Intermediate P-State #6		N/A	N/A	N/A
VID_VDD	1			
IDD Max				
Thermal Design Power	2,3			
Min P-State		800 MHz	800 MHz	800 MHz
VID_VDD	1	0.800 V	0.800 V	0.800 V
IDD Max		8.00 A	8.00 A	8.00 A
Thermal Design Power	2,3	9.4 W	9.4 W	9.4 W
Halt/Stop Grant				
IDDC1 Max @ Max P-State	4	7.36 A	7.36 A	7.35 A
IDDC1 Max @ Min P-State	5	1.50 A	1.50 A	1.50 A
I/O Power	7,8	3.0 W	3.0 W	3.0 W
C1E/S1 Min P-State VID_VDD	9			
IDDC1E Max		0.88 A	0.88 A	0.88 A
I/O Power	7,8	350 mW	350 mW	350 mW
C1E/S1 AltVID	12			
VID_VDD	13,	0.750 V	0.750 V	0.750 V
IDDC1E Max		0.67 A	0.67 A	0.67 A
I/O Power	7,8	350 mW	350 mW	350 mW
S3	10			
I/O Power	7,8,11	200 mW	200 mW	200 mW

The notes for this table are on page 43.

Parameter/OPN	Notes	TMDTL68HAX5DM		
Tdie Max		95°C		
Tambient		0°C to 35°C		
Trise		10°C		
Thermal Resistance (die-amb)		1.43°C/W		
Max P-State		2400 MHz		
VID_VDD	1	1.075 V	1.100 V	1.125 V
IDD Max		29.77 A		
Thermal Design Power	2,3	35.0 W		
Intermediate P-State #1		2200 MHz		
VID_VDD	1	1.050 V	1.075 V	1.100 V
IDD Max		26.67 A		
Thermal Design Power	2,3	31.0 W		
Intermediate P-State #2		2000 MHz		
VID_VDD	1	1.025 V	1.050 V	1.075 V
IDD Max		23.71 A		
Thermal Design Power	2,3	27.3 W		
Intermediate P-State #3		1800 MHz		
VID_VDD	1	1.000 V	1.025 V	1.050 V
IDD Max		20.90 A		
Thermal Design Power	2,3	23.9 W		
Intermediate P-State #4		1600 MHz		
VID_VDD	1	0.975 V	1.000 V	1.025 V
IDD Max		18.26 A		
Thermal Design Power	2,3	20.8 W		
Intermediate P-State #5		N/A		
VID_VDD	1			
IDD Max				
Thermal Design Power	2,3			
Intermediate P-State #6		N/A		
VID_VDD	1			
IDD Max				
Thermal Design Power	2,3			
Min P-State		800 MHz		
VID_VDD	1	0.800 V		
IDD Max		8.00 A		
Thermal Design Power	2,3	9.4 W		
Halt/Stop Grant				
IDDC1 Max @ Max P-State	4	7.36 A		
IDDC1 Max @ Min P-State	5	1.50 A		
I/O Power	7,8	3.0 W		
C1E/S1 Min P-State VID_VDD	9			
IDDC1E Max		0.88 A		
I/O Power	7,8	350 mW		
C1E/S1 AltVID	12			
VID_VDD	13,	0.750 V		
IDDC1E Max		0.67 A		
I/O Power	7,8	350 mW		
S3	10			
I/O Power	7,8,11	200 mW		

The notes for this table are on page 43.

AMD Turion™ 64 X2 Mobile Technology Thermal and Power Specification Table Notes:

1. The VID_VDD voltage is the VID[5:0] requested VDD supply level. Refer to the BIOS and Kernel Developer's Guide for AMD NPT Family Processors, order #32559, for details.
2. Thermal Design Power (TDP) is measured under the conditions of Tdie Max, IDD Max, and VDD=VID_VDD, and include all power dissipated on-die from VDD, VDDIO, VLDT, VTT, and VDDA. Contact your Field Application Engineer for more information on TDP specifications.
3. Thermal Design Power (TDP) specifications for dual core processors assume equivalent P-states (Voltage and frequency) and equivalent Tcase conditions for both cores. Refer to the BIOS and Kernel Developer's Guide for AMD NPT Family Processors, order #32559, for details on P-state operation for dual core processors.
4. Assumes Tdie max, max P-state VID_VDD +25 mV, clock divider set to 512.
5. Assumes 50°C, min P-state VID_VDD +50 mV, clock divider set to 512.
6. IDDC1 specifications for dual core processors assume equivalent Voltage, clock divisor, and Tcase conditions for both cores.
7. Thermal Design Power dissipated by the processor VDDIO, VTT, VLDT, and VDDA power planes only.
8. Assumes VDDIO = 1.8 V and VTT = VDDIO / 2.
9. Assumes 35°C, min P-state VID_VDD, clock divider set to 512, HyperTransport™ links disconnected, memory in self-refresh mode, DDR SDRAM interface tri-stated except CKE pins.
10. Assumes 35°C, VDD, VDDA, and VLDT supplies are off, VDDIO and VTT are powered, memory in self-refresh mode and DDR SDRAM interface tri-stated except CKE pins.
11. Thermal Design Power dissipated by the processor VDDIO and VTT power planes only.
12. Assumes 35°C, AltVID, clock divider set to 512, HyperTransport™ links disconnected, memory in self-refresh mode, DDR SDRAM interface tri-stated except CKE pins. Not all systems are AltVID capable. Refer to the BIOS and Kernel Developer's Guide for AMD NPT Family Processors, order #32559, for further details.
13. BIOS programs the AltVID setting. Not all systems are AltVID capable. Refer to the BIOS and Kernel Developer's Guide for AMD NPT Family Processors, order #32559 for further details.

5 AMD Athlon™ 64 X2 Dual-Core Processor

The following sections contain the OPN description and thermal and power specifications for the AMD Athlon™ 64 X2 dual-core processor. Each column in the thermal and power tables represents a specific Ordering Part Number (OPN). Section 5.1 provides an example of the OPN structure for this processor family.

5.1 AMD Athlon™ 64 X2 Dual-Core Processor Ordering Part Number Description

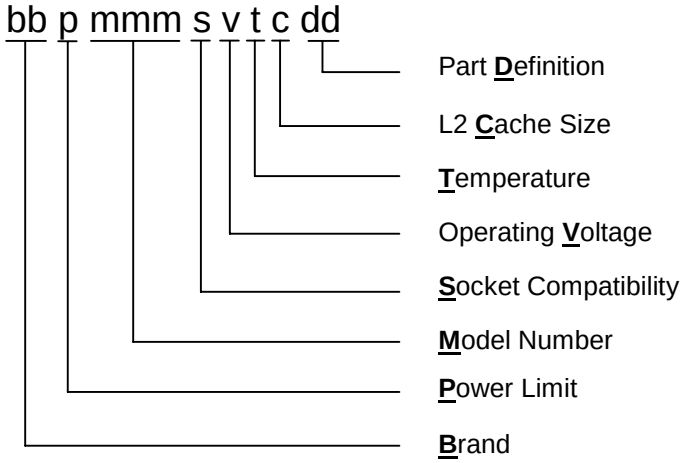


Figure 7. AMD Athlon™ 64 X2 Dual-Core Processor Subsection Ordering Part Number Diagram

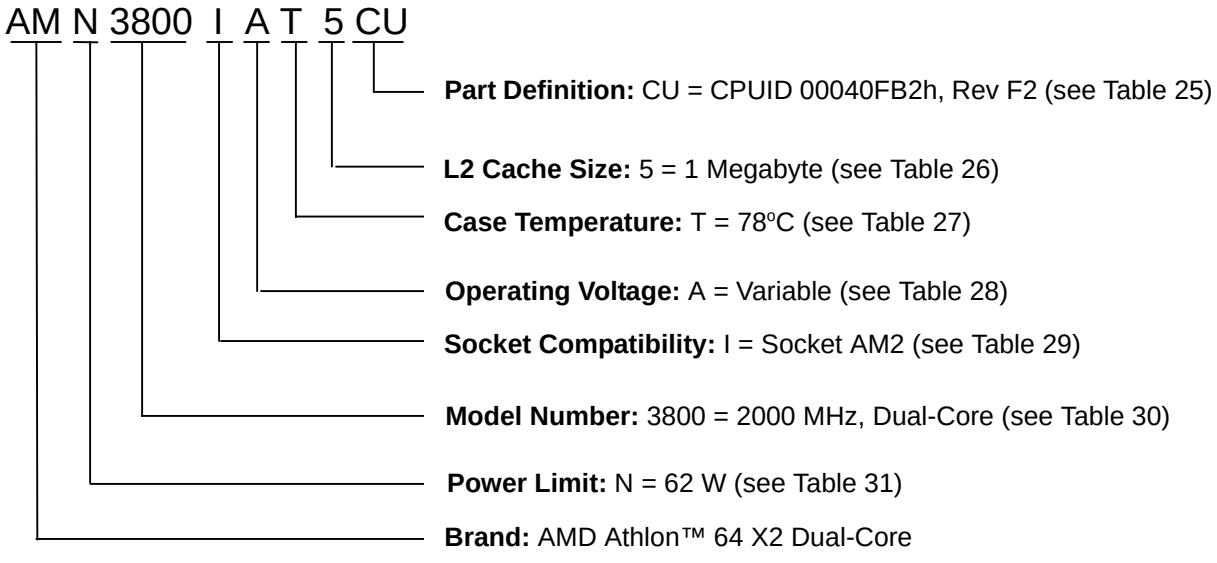


Figure 8. AMD Athlon™ 64 X2 Dual-Core Ordering Part Number Example

Table 25: AMD Athlon™ 64 X2 Dual-Core Processor Part Definition Options

Part Definition	Revision	CPUID 8000_0001h EAX [31:0] (CPUID)	Package Drawing
CU	Rev F2	00040FB2h	Lidded
CT	Rev F2	00040F82h	Lidless H2
DC	Rev G1	00060F81h	Lidless H4
DM	Rev G2	00060F82h	Lidless H4

Table 26: AMD Athlon™ 64 X2 Dual-Core Processor L2 Cache Size Options

OPN Character	Cache Size
5	1 MB
4	512 KB

Table 27: AMD Athlon™ 64 X2 Dual-Core Processor Temperature Options

OPN Character	Temperature
T	78° C
X	95° C

Table 28: AMD Athlon™ 64 X2 Dual-Core Processor Operating Voltage

OPN Character	Operating Voltage
A	Variable

Table 29: AMD Athlon™ 64 X2 Dual-Core Processor Package Options

OPN Character	Package
I	Socket AM2 Processor
H	Socket S1 Processor

Table 30: AMD Athlon™ 64 X2 Dual-Core Processor Model Number Options

Package	Cache Size	Frequency	Model Number
Socket AM2 Processor	1 MB	2000 MHz	3800+
Socket AM2 Processor	1 MB	2200 MHz	4200+
Socket AM2 Processor	1 MB	2400 MHz	4600+
Socket S1 Processor	512 KB	1700 MHz	TK53
Socket S1 Processor	512 KB	1800 MHz	TK55
Socket S1 Processor	512 KB	1900 MHz	TK57

Table 31: AMD Athlon™ 64 X2 Dual-Core Processor Power Limit

OPN Character	Power Limit
D	35 W
N	62 W

5.2 AMD Athlon™ 64 X2 Dual-Core Processor Thermal and Power Table Guide

The Thermal and Power Table Guide shown in Table 32 maps SOPNs and the properties associated with their defined characters to the proper thermal and power table subsections and page numbers. This table is designed to be used as a quick reference for finding the appropriate subsection for the thermal and power tables corresponding to an SOPN.

Table 32: AMD Athlon™ 64 X2 Dual-Core Thermal and Power Table Guide

SOPN	Power	Revision	Dual-Core	Thermal/Power Tables
AMN mmmmsvtc **CU**	62 W	Rev F2	Dual-Core	Section 5.3.1 on page 49
AMD mmmmsvtc **DC**	35 W	Rev G1	Dual-Core	Section 5.3.2 on page 50
AMD mmmmsvtc **DM**	35 W	Rev G2	Dual-Core	Section 5.3.3 on page 51
AMD mmmmsvtc **CT**	35 W	Rev F2	Dual-Core	Section 5.3.4 on page 52

5.3 AMD Athlon™ 64 X2 Dual-Core Processor Thermal and Power Specifications

The thermal and power specification tables contain the thermal and power requirements for each OPN. This includes the information necessary for thermal management (for example, heat sink requirements, temperature assumptions) and power delivery (for example, voltage, current, and power dissipation for each P-state). For all other electrical specifications for the processor, refer to the *AMD NPT Family 0Fh Processor Electrical Data Sheet*, order #31119. For power management BIOS requirements, refer to the *BIOS and Kernel Developer's Guide for AMD NPT Family 0Fh Processors*, order #32559.

Section 5.1 on page 44 provides an example of the OPN structure for processors documented in this chapter and Table 32 on page 47 provides a guide to OPN organization in the following subsections. Refer to Section 1.2 on page 11 and Section 1.3 on page 12 for numbering conventions and terminology definitions used in these tables.

5.3.1 AMN mmmmsvtc CU 62W, AM2, Mobile, Rev F2 Thermal and Power Specifications

Parameter/OPN	Notes	AMN3800IAT5CU		AMN4200IAT5CU	
Tcase Max		78°C		78°C	
Tambient		0°C to 35°C		0°C to 35°C	
Trise		5°C		5°C	
Thermal Resistance (die-amb)		0.61°C/W		0.61°C/W	
Max P-State		2000 MHz		2200 MHz	
VID_VDD	1	1.200 V	1.250 V	1.200 V	1.250 V
IDD Max		49.17 A		49.17 A	
Thermal Design Power	2,3	62.0 W		62.0 W	
Intermediate P-State #1		1800 MHz		2000 MHz	
VID_VDD	1	1.150 V	1.200 V	1.150 V	1.200 V
IDD Max		41.65 A		41.83 A	
Thermal Design Power	2,3	50.9 W		51.1 W	
Intermediate P-State #2		1600 MHz		1800 MHz	
VID_VDD	1	1.100 V	1.150 V	1.100 V	1.150 V
IDD Max		35.36 A		35.36 A	
Thermal Design Power	2,3	41.9 W		41.9 W	
Intermediate P-State #3		N/A		1600 MHz	
VID_VDD	1			1.050 V	1.100 V
IDD Max				32.10 A	
Thermal Design Power	2,3			36.7 W	
Intermediate P-State #4		N/A		N/A	
VID_VDD	1				
IDD Max					
Thermal Design Power	2,3				
Intermediate P-State #5		N/A		N/A	
VID_VDD	1				
IDD Max					
Thermal Design Power	2,3				
Intermediate P-State #6		N/A		N/A	
VID_VDD	1				
IDD Max					
Thermal Design Power	2,3				
Min P-State		800 MHz		800 MHz	
VID_VDD	1	0.950 V		0.950 V	
IDD Max		14.63 A		12.63 A	
Thermal Design Power	2,3	16.9 W		15.0 W	
Halt/Stop Grant					
IDDC1 Max @ Max P-State	4	20.92 A		18.06 A	
IDDC1 Max @ Min P-State	5	4.00 A		3.49 A	
I/O Power	7,8	3.0 W		3.0 W	
C3/S1 Min P-State VID_VDD	9				
IDDC3 Max		2.52 A		2.52 A	
I/O Power	7,8	1.2 W		1.2 W	
S3	10				
I/O Power	7,8,11	250 mW		250 mW	

The notes for this table are on page 53.

5.3.2 AMD mmmmsvtc DC 35W, S1, Mobile, Rev G1 Thermal and Power Specifications

Parameter/OPN	Notes	AMDTK53HAX4DC			AMDTK55HAX4DC		
Tdie Max		95°C			95°C		
Tambient		0°C to 35°C			0°C to 35°C		
Trise		10°C			10°C		
Thermal Resistance (die-amb)		1.61°C/W			1.61°C/W		
Max P-State		1700 MHz			1800 MHz		
VID_VDD	1	1.075 V	1.100 V	1.125 V	1.075 V	1.100 V	1.125 V
IDD Max		26.05 A			26.05 A		
Thermal Design Power	2,3	31.0 W			31.0 W		
Intermediate P-State #1		1600 MHz			1600 MHz		
VID_VDD	1	1.050 V	1.075 V	1.100 V	1.050 V	1.075 V	1.100 V
IDD Max		23.81 A			22.95 A		
Thermal Design Power	2,3	28.0 W			27.1 W		
Intermediate P-State #2		N/A			N/A		
VID_VDD	1						
IDD Max							
Thermal Design Power	2,3						
Intermediate P-State #3		N/A			N/A		
VID_VDD	1						
IDD Max							
Thermal Design Power	2,3						
Intermediate P-State #4		N/A			N/A		
VID_VDD	1						
IDD Max							
Thermal Design Power	2,3						
Intermediate P-State #5		N/A			N/A		
VID_VDD	1						
IDD Max							
Thermal Design Power	2,3						
Intermediate P-State #6		N/A			N/A		
VID_VDD	1						
IDD Max							
Thermal Design Power	2,3						
Min P-State		800 MHz			800 MHz		
VID_VDD	1	0.900 V			0.900 V		
IDD Max		11.00 A			11.00 A		
Thermal Design Power	2,3	12.9 W			12.9 W		
Halt/Stop Grant							
IDDC1 Max @ Max P-State	4	9.05 A			8.82 A		
IDDC1 Max @ Min P-State	5	2.60 A			2.60 A		
I/O Power	7,8	3.0 W			3.0 W		
C1E/S1 Min P-State VID_VDD	9						
IDDC1E Max		1.72 A			1.72 A		
I/O Power	7,8	500 mW			500 mW		
S3	10						
I/O Power	7,8,11	250 mW			250 mW		

The notes for this table are on page 53.

5.3.3 AMD mmmmsvtc DM 35W, S1, Mobile, Rev G2 Thermal and Power Specifications

Parameter/OPN	Notes	AMDTK57HAX4DM		
Tdie Max		95°C		
Tambient		0°C to 35°C		
Trise		10°C		
Thermal Resistance (die-amb)		1.61°C/W		
Max P-State		1900 MHz		
VID_VDD	1	1.075 V	1.100 V	1.125 V
IDD Max		26.05 A		
Thermal Design Power	2,3	31.0 W		
Intermediate P-State #1		1800 MHz		
VID_VDD	1	1.050 V	1.075 V	1.100 V
IDD Max		23.90 A		
Thermal Design Power	2,3	28.1 W		
Intermediate P-State #2		1600 MHz		
VID_VDD	1	1.025 V	1.050 V	1.075 V
IDD Max		20.98 A		
Thermal Design Power	2,3	24.5 W		
Intermediate P-State #3		N/A		
VID_VDD	1			
IDD Max				
Thermal Design Power	2,3			
Intermediate P-State #4		N/A		
VID_VDD	1			
IDD Max				
Thermal Design Power	2,3			
Intermediate P-State #5		N/A		
VID_VDD	1			
IDD Max				
Thermal Design Power	2,3			
Intermediate P-State #6		N/A		
VID_VDD	1			
IDD Max				
Thermal Design Power	2,3			
Min P-State		800 MHz		
VID_VDD	1	0.900 V		
IDD Max		11.00 A		
Thermal Design Power	2,3	12.9 W		
Halt/Stop Grant				
IDDC1 Max @ Max P-State	4	9.05 A		
IDDC1 Max @ Min P-State	5	2.60 A		
I/O Power	7,8	3.0 W		
C1E/S1 Min P-State VID_VDD	9			
IDDC1E Max		1.72 A		
I/O Power	7,8	500 mW		
S3	10			
I/O Power	7,8,11	250 mW		

The notes for this table are on page 53.

5.3.4 AMD mmmmsvtc CT 35W, S1, Mobile, Rev F2 Thermal and Power Specifications

Parameter/OPN	Notes	AMDTK55HAX4CT	
Tdie Max		95°C	
Tambient		0°C to 35°C	
Trise		10°C	
Thermal Resistance (die-amb)		1.43°C/W	
Max P-State		1800 MHz	
VID_VDD	1	1.075 V	1.100 V
IDD Max		29.77 A	
Thermal Design Power	2,3	35.0 W	
Intermediate P-State #1		1600 MHz	
VID_VDD	1	1.025 V	1.050 V
IDD Max		24.98 A	
Thermal Design Power	2,3	28.6 W	
Intermediate P-State #2		N/A	
VID_VDD	1		
IDD Max			
Thermal Design Power	2,3		
Intermediate P-State #3		N/A	
VID_VDD	1		
IDD Max			
Thermal Design Power	2,3		
Intermediate P-State #4		N/A	
VID_VDD	1		
IDD Max			
Thermal Design Power	2,3		
Intermediate P-State #5		N/A	
VID_VDD	1		
IDD Max			
Thermal Design Power	2,3		
Intermediate P-State #6		N/A	
VID_VDD	1		
IDD Max			
Thermal Design Power	2,3		
Min P-State		800 MHz	
VID_VDD	1	0.900 V	
IDD Max		12.22 A	
Thermal Design Power	2,3	14.0 W	
Halt/Stop Grant			
IDDC1 Max @ Max P-State	4	8.08 A	
IDDC1 Max @ Min P-State	5	2.56 A	
I/O Power	7,8	3.0 W	
C1E/S1 Min P-State VID_VDD	9		
IDDC1E Max		1.67 A	
I/O Power	7,8	500 mW	
S3	10		
I/O Power	7,8,11	250 mW	

The notes for this table are on page 53.

AMD Athlon™ 64 X2 Dual-Core Processor Thermal and Power Specification Table Notes:

1. The VID_VDD voltage is the VID[5:0] requested VDD supply level. Refer to the BIOS and Kernel Developer's Guide for AMD NPT Family Processors, order #32559, for details.
2. Thermal Design Power (TDP) is measured under the conditions of Tdie Max, IDD Max, and VDD=VID_VDD, and include all power dissipated on-die from VDD, VDDIO, VLDT, VTT, and VDDA. Contact your Field Application Engineer for more information on TDP specifications.
3. Thermal Design Power (TDP) specifications for dual core processors assume equivalent P-states (Voltage and frequency) and equivalent Tcase conditions for both cores. Refer to the BIOS and Kernel Developer's Guide for AMD NPT Family Processors, order #32559, for details on P-state operation for dual core processors.
4. Assumes Tdie max, max P-state VID_VDD +25 mV, clock divider set to 512.
5. Assumes 50°C, min P-state VID_VDD +50 mV, clock divider set to 512.
6. IDDC1 specifications for dual core processors assume equivalent Voltage, clock divisor, and Tcase conditions for both cores.
7. Thermal Design Power dissipated by the processor VDDIO, VTT, VLDT, and VDDA power planes only.
8. Assumes VDDIO = 1.8 V and VTT = VDDIO / 2.
9. Assumes 35°C, min P-state VID_VDD, clock divider set to 512, HyperTransport™ links disconnected, memory in self-refresh mode, DDR SDRAM interface tri-stated except clocks and CKE pins.
10. Assumes 35°C, VDD, VDDA, and VLDT supplies are off, VDDIO and VTT are powered, memory in self-refresh mode and DDR SDRAM interface tri-stated except CKE pins.
11. Thermal Design Power dissipated by the processor VDDIO and VTT power planes only.

6 AMD Embedded Mobile Processor

The following sections contain the OPN description and thermal and power specifications for the AMD Embedded Processors. Each column in the thermal and power tables represents a specific Ordering Part Number (OPN). Section 6.1 provides an example of the OPN structure for this processor family.

6.1 AMD Embedded Mobile Processor Ordering Part Number Description

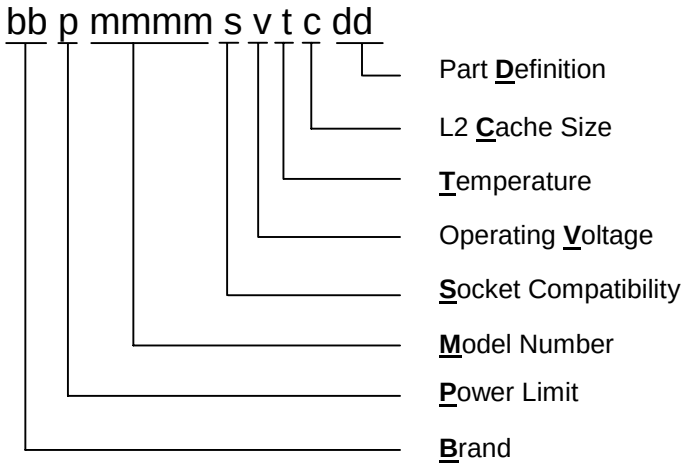


Figure 9. AMD Embedded Mobile Processor Ordering Part Number Diagram

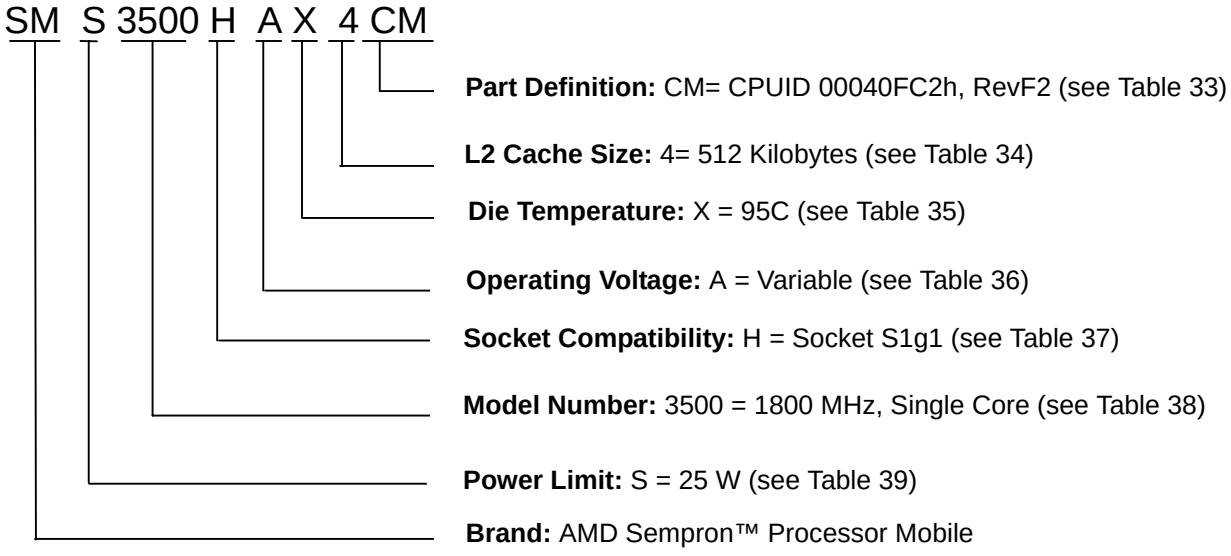


Figure 10. AMD Embedded Mobile Processor Ordering Part Number Example

Table 33. AMD Embedded Mobile Processor Part Definition Options

Part Definition	Revision	CPUID 8000_0001h EAX [31:0] (CPUID)	Package Drawing
CM	Rev F2	00040FC2h	Lidless H3
CT	Rev F2	00040F82h	Lidless H2
DM	Rev G2	00060F82h	Lidless H4
DQ	Rev G2	00060FC2h	Lidless H5

Table 34. AMD Embedded Mobile Processor L2 Cache Size Options

OPN Character	Cache Size
3	256 KB
4	512 KB
5	1 MB

Table 35. AMD Embedded Mobile Processor Temperature Options

OPN Character	Temperature
X	95ºC

Table 36. AMD Embedded Mobile Processor Operating Voltage

OPN Character	Operating Voltage
A	Variable

Table 37. AMD Embedded Mobile Processor Package Options

OPN Character	Package
H	Socket S1g1 Processor

Table 38. AMD Embedded Mobile Processor Model Number Options

Package	Cache Size	Frequency	Model Number
Socket S1g1 Processor	256 KB	1000 MHz	2100+
Socket S1g1 Processor	512 KB	1800 MHz	3500+
Socket S1g1 Processor	512 KB	2000 MHz	3700+
Socket S1g1 Processor	1 MB	1600 MHz	TL52
Socket S1g1 Processor	1 MB	1800 MHz	TL56
Socket S1g1 Processor	1 MB	2100 MHz	TL62

Table 39. AMD Embedded Mobile Processor Power Limit

OPN Character	Power Limit
D	35 W
F	8 W
S	25 W

6.2 AMD Embedded Mobile Processor Thermal and Power Table Guide

The thermal and power table guide shown in Table 40 maps SOPNs and the properties associated with their defined characters to the proper thermal and power table subsections and page numbers. This table is designed to be used as a quick reference for finding the appropriate subsection for the thermal and power tables corresponding to an SOPN.

Table 40. AMD Embedded Mobile Processor Thermal and Power Table Guide

SOPN	Power	Revision	Single/Dual-Core	Thermal/Power Tables
SMS mmmmsvtc **CM**	25 W	Rev F2	Single Core	Section 6.2.1 on page 58
SMS mmmmsvtc **DQ**	25 W	Rev G2	Single Core	Section 6.2.2 on page 59
SMF mmmmsvtc **DQ**	8 W	Rev G2	Single Core	Section 6.2.3 on page 60
TMD mmmmsvtc **CT**	35 W	Rev F2	Dual Core	Section 6.2.4 on page 61
TMD mmmmsvtc **DM**	35 W	Rev G2	Dual Core	Section 6.2.5 on page 62

6.2.1 SMS mmmmsvtc CM 25W, S1, Embedded Mobile, Rev F2 Thermal and Power Specifications

Parameter/OPN	Notes	SMS3500HAX4CM		
Tdie Max		95°C		
Tambient		0°C to 35°C		
Max P-State		1800 MHz		
VID_VDD	1	1.125 V	1.150 V	1.200 V
IDD Max		19.6 A		
Thermal Design Power	2,3	25.0 W		
Intermediate P-State #1		1600 MHz		
VID_VDD	1	1.075 V	1.100 V	1.150 V
IDD Max		16.4 A		
Thermal Design Power	2,3	20.6 W		
Intermediate P-State #2		N/A		
VID_VDD	1			
IDD Max				
Thermal Design Power	2,3			
Intermediate P-State #3		N/A		
VID_VDD	1			
IDD Max				
Thermal Design Power	2,3			
Intermediate P-State #4		N/A		
VID_VDD	1			
IDD Max				
Thermal Design Power	2,3			
Intermediate P-State #5		N/A		
VID_VDD	1			
IDD Max				
Thermal Design Power	2,3			
Intermediate P-State #6		N/A		
VID_VDD	1			
IDD Max				
Thermal Design Power	2,3			
Min P-State		800 MHz		
VID_VDD	1	0.950 V		
IDD Max		8.4 A		
Thermal Design Power	2,3	11.0 W		
Halt/Stop Grant				
IDDC1 Max @ Max P-State	4	8.0 A		
IDDC1 Max @ Min P-State	5	2.5 A		
I/O Power	7,8	3.0 W		
C3/S1 Min P-State VID_VDD	9			
IDDC3 Max	10	N/A		
I/O Power	7,8	N/A		
C3/S1 AltVID		N/A		
VID_VDD		N/A		
IDDC3 Max				
I/O Power				
S3	10			
I/O Power	7,8,11	250 mW		

The notes for this table are on page 63.

6.2.2 SMS mmmmsvtc DQ 25W, S1, Embedded Mobile, Rev G2 Thermal and Power Specifications

Parameter/OPN	Notes	SMS3700HAX4DQ		
Tdie Max		95°C		
Minimum Tambient		0°C		
Max P-State		2000 MHz		
VID_VDD	1	1.150 V	1.200 V	1.250 V
IDD Max		19.1 A		
Thermal Design Power	2,3	25.0 W		
Intermediate P-State #1		1800 MHz		
VID_VDD	1	1.125 V	1.175 V	1.225 V
IDD Max		17.1 A		
Thermal Design Power	2,3	22.2 W		
Intermediate P-State #2		1600 MHz		
VID_VDD	1	1.100 V	1.150 V	1.200 V
IDD Max		15.2 A		
Thermal Design Power	2,3	19.7 W		
Intermediate P-State #3		N/A		
VID_VDD	1			
IDD Max				
Thermal Design Power	2,3			
Intermediate P-State #4		N/A		
VID_VDD	1			
IDD Max				
Thermal Design Power	2,3			
Intermediate P-State #5		N/A		
VID_VDD	1			
IDD Max				
Thermal Design Power	2,3			
Intermediate P-State #6		N/A		
VID_VDD	1			
IDD Max				
Thermal Design Power	2,3			
Min P-State		800 MHz		
VID_VDD	1	0.950 V		
IDD Max		11.6 A		
Thermal Design Power	2,3	14.0 W		
Halt/Stop Grant				
IDDC1 Max @ Max P-State	4	10.2 A		
IDDC1 Max @ Min P-State	5	2.5 A		
I/O Power	7,8	3.0 W		
C3/S1 Min P-State VID_VDD	9			
IDDC3 Max	10	2.4 A		
I/O Power	7,8	1.2 W		
C3/S1 AltVID				
VID_VDD		N/A		
IDDC3 Max		N/A		
I/O Power		N/A		
S3	10			
I/O Power	7,8,11	250 mW		

The notes for this table are on page 63.

6.2.3 SMF mmmmsvtc DQ 8W, S1, Embedded Mobile, Rev G2 Thermal and Power Specifications

Parameter/OPN	Notes	SMF2100HAX3DQ		
Tdie Max		95°C		
Minimum Tambient		0°C		
Max P-State		1000 MHz		
VID_VDD	1	0.850 V	0.875 V	0.900 V
IDD Max		5.9 A		
Thermal Design Power	2,3	8.0 W		
Intermediate P-State #1		N/A		
VID_VDD	1			
IDD Max				
Thermal Design Power	2,3			
Intermediate P-State #2		N/A		
VID_VDD	1			
IDD Max				
Thermal Design Power	2,3			
Intermediate P-State #3		N/A		
VID_VDD	1			
IDD Max				
Thermal Design Power	2,3			
Intermediate P-State #4		N/A		
VID_VDD	1			
IDD Max				
Thermal Design Power	2,3			
Intermediate P-State #5		N/A		
VID_VDD	1			
IDD Max				
Thermal Design Power	2,3			
Intermediate P-State #6		N/A		
VID_VDD	1			
IDD Max				
Thermal Design Power	2,3			
Min P-State		N/A		
VID_VDD	1			
IDD Max				
Thermal Design Power	2,3			
Halt/Stop Grant				
IDDC1 Max @ Max P-State	4	3.2 A		
IDDC1 Max @ Min P-State	5	N/A		
I/O Power	7,8	3.0 W		
C3/S1 Min P-State VID_VDD	9			
IDDC3 Max	10	N/A		
I/O Power	7,8	N/A		
C3/S1 AltVID				
VID_VDD		N/A		
IDDC3 Max		N/A		
I/O Power		N/A		
S3	10			
I/O Power	7,8,11	250 mW		

The notes for this table are on page 63.

6.2.4 **TMD** mmmmsvtc **CT 35W, S1, Embedded Mobile, Rev F2 Thermal and Power Specifications**

Parameter/OPN	**Notes**	**TMDTL52HAX5CT**	
Tdie Max		95°C	
Tambient		0°C to 35°C	
Max P-State		1600 MHz	
VID_VDD	1	1.075 V	1.100 V
IDD Max		26.05 A	
Thermal Design Power	2,3	31.0 W	
Intermediate P-State #1		N/A	
VID_VDD	1		
IDD Max			
Thermal Design Power	2,3		
Intermediate P-State #2		N/A	
VID_VDD	1		
IDD Max			
Thermal Design Power	2,3		
Intermediate P-State #3		N/A	
VID_VDD	1		
IDD Max			
Thermal Design Power	2,3		
Intermediate P-State #4		N/A	
VID_VDD	1		
IDD Max			
Thermal Design Power	2,3		
Intermediate P-State #5		N/A	
VID_VDD	1		
IDD Max			
Thermal Design Power	2,3		
Intermediate P-State #6		N/A	
VID_VDD	1		
IDD Max			
Thermal Design Power	2,3		
Min P-State		800 MHz	
VID_VDD	1	0.800 V	
IDD Max		10.00 A	
Thermal Design Power	2,3	11.0 W	
Halt/Stop Grant			
IDDC1 Max @ Max P-State	4	6.81 A	
IDDC1 Max @ Min P-State	5	1.88 A	
I/O Power	7,8	3.0 W	
C1E/S1 Min P-State VID_VDD	9		
IDDC1E Max		0.88 A	
I/O Power	7,8	350 mW	
C1E/S1 AltVID	12		
VID_VDD	13	0.750 V	
IDDC1E Max		0.67 A	
I/O Power	7,8	350 mW	
S3	10		
I/O Power	7,8,11	250 mW	

The notes for this table are on page 63.

6.2.5 TMD mmmmsvtc DM 35W, S1, Embedded Mobile, Rev G2 Thermal and Power Specifications

Parameter/OPN	Notes	TMDTL56HAX5DM			TMDTL62HAX5DM		
Tdie Max		95°C			95°C		
Tambient		0°C to 35°C			0°C to 35°C		
Max P-State		1800 MHz			2100 MHz		
VID_VDD	1	1.075 V	1.100 V	1.125 V	1.075 V	1.100 V	1.125 V
IDD Max		26.05 A			29.77 A		
Thermal Design Power	2,3	31.0 W			35.0 W		
Intermediate P-State #1		1600 MHz			2000 MHz		
VID_VDD	1	1.050 V	1.075 V	1.100 V	1.050 V	1.075 V	1.100 V
IDD Max		22.95 A			25.81 A		
Thermal Design Power	2,3	27.1 W			30.1 W		
Intermediate P-State #2		N/A			1800 MHz		
VID_VDD	1				1.025 V	1.050 V	1.075 V
IDD Max					22.83 A		
Thermal Design Power	2,3				26.4 W		
Intermediate P-State #3		N/A			1600 MHz		
VID_VDD	1				1.000 V	1.025 V	1.050 V
IDD Max					20.00 A		
Thermal Design Power	2,3				23.0 W		
Intermediate P-State #4		N/A			N/A		
VID_VDD	1						
IDD Max							
Thermal Design Power	2,3						
Intermediate P-State #5		N/A			N/A		
VID_VDD	1						
IDD Max							
Thermal Design Power	2,3						
Intermediate P-State #6		N/A			N/A		
VID_VDD	1						
IDD Max							
Thermal Design Power	2,3						
Min P-State		800 MHz			800 MHz		
VID_VDD	1	0.800 V			0.800 V		
IDD Max		8.00 A			8.00 A		
Thermal Design Power	2,3	9.4 W			9.4 W		
Halt/Stop Grant							
IDDC1 Max @ Max P-State	4	6.70 A			7.36 A		
IDDC1 Max @ Min P-State	5	1.50 A			1.50 A		
I/O Power	7,8	3.0 W			3.0 W		
C1E/S1 Min P-State VID_VDD	9						
IDDC1E Max		0.88 A			0.88 A		
I/O Power	7,8	350 mW			350 mW		
C1E/S1 AltVID	12						
VID_VDD	13	0.750 V			0.750 V		
IDDC1E Max		0.67 A			0.67 A		
I/O Power	7,8	350 mW			350 mW		
S3	10						
I/O Power	7,8,11	200 mW			200 mW		

The notes for this table are on page 63.

AMD Embedded Thermal and Power Specification Table Notes

1. The VID_VDD voltage is the VID[5:0] requested VDD supply level. Refer to the BIOS and Kernel Developer's Guide for AMD NPT Family Processors, order #32559, for details.
2. Thermal Design Power (TDP) is measured under the conditions of Tdie Max, IDD Max, and VDD=VID_VDD, and include all power dissipated on-die from VDD, VDDIO, VLDT, VTT, and VDDA. Contact your Field Application Engineer for more information on TDP specifications.
3. Thermal Design Power (TDP) specifications for dual core processors assume equivalent P-states (Voltage and frequency) and equivalent Tcase conditions for both cores. Refer to the BIOS and Kernel Developer's Guide for AMD NPT Family Processors, order #32559, for details on P-state operation for dual core processors.
4. Assumes Tdie max, max P-state VID_VDD +25 mV, clock divider set to 512.
5. Assumes 50°C, min P-state VID_VDD +50 mV, clock divider set to 512.
6. IDDC1 specifications for dual core processors assume equivalent Voltage, clock divisor, and Tcase conditions for both cores.
7. Thermal Design Power dissipated by the processor VDDIO, VTT, VLDT, and VDDA power planes only.
8. Assumes VDDIO = 1.8 V and VTT = VDDIO / 2.
9. Assumes 35°C, min P-state VID_VDD, clock divider set to 512, HyperTransport™ links disconnected, memory in self-refresh mode, DDR SDRAM interface tri-stated except clocks and CKE pins.
10. Assumes 35°C, VDD, VDDA, and VLDT supplies are off, VDDIO and VTT are powered, memory in self-refresh mode and DDR SDRAM interface tri-stated except CKE pins.
11. Thermal Design Power dissipated by the processor VDDIO and VTT power planes only.
12. Assumes 35°C, AltVID, clock divider set to 512, HyperTransport™ links disconnected, memory in self-refresh mode, DDR SDRAM interface tri-stated except CKE pins. Not all systems are AltVID capable. Refer to the BIOS and Kernel Developer's Guide for AMD NPT Family Processors, order #32559, for further details.
13. BIOS programs the AltVID setting. Not all systems are AltVID capable. Refer to the BIOS and Kernel Developer's Guide for AMD NPT Family Processors, order #32559 for further details.

7 Power Supply Specifications

7.1 bbpmmmm **I** vtcdd **- Socket AM2 Power Supply Operating Conditions**

Table 41. bbpmmmm **I** vtcdd **VDD Power Supply DC Operating Conditions**

Symbol	Parameter	Units	Min	Typ	Max	Notes
VID_VDD	VID Requested VDD Supply Level	V	Refer to the thermal/power and BIOS tables under the appropriate SOPN section for this OPN specific parameter.			1
VDD_dc	VDD Supply Voltage	V	VID_VDD – 50 mV	VID_VDD	VID_VDD + 50 mV	
VDD_PON	VDD Supply Voltage before PWROK assertion during power-on.	V	1.050 V	1.100 V	MaxVID	2, 3
IDD	VDD Power Supply Current	A	Refer to the thermal/power tables under the appropriate SOPN section for this OPN specific parameter.			

Notes:

1) The processor drives a VID code corresponding to this voltage.

2) The processor's VID[5:0] outputs select VDD_PON nom before PWROK is asserted. Transients up to MaxVID are allowed.

3) MaxVID is reported in MSRC001_0042 (FIDVID_STATUS).

Table 42. bbpmmmm **I** vtcdd **VDD Power Supply AC Operating Conditions**

Symbol	Parameter	Units	Min	Typ	Max	Notes
VDD_ac	VDD Supply Voltage	V	VID_VDD – 140 mV	VID_VDD	VID_VDD + 150 mV	1

Notes:

1) Transient duration below VDD_dc min is limited to < 5µs. Transient duration above VDD_dc max is limited to < 10% duty cycle. Test by probing differentially at COREFB_H and COREFB_L with 20MHz scope bandwidth limit.

Table 43. bbpmmmm **I** vtcdd **Non-VDD Power Supply AC and DC Operating Conditions**

Symbol	Parameter	Units	Min	Typ	Max	Notes
VDDIO_dc	VDDIO Supply Voltage for DDR2 electricals	V	1.7	1.8	1.9	7
VDDIO_dc	VDDIO Supply Voltage for DDR2 electricals for OPN ADO3600IAA5DL	V	1.77	1.8	1.9	7
VDDIO_ac	VDDIO supply voltage	V	VDDIO_dc – 150 mV		VDDIO_dc + 150 mV	5, 6
VLDT	VLDT Supply Voltage	V	1.14	1.2	1.26	
VTT_dc	VTT Supply Voltage for DDR2 electricals	V	0.85	0.9	0.95	8
VTT_ac	VTT Supply Voltage	V	VTT_dc – 75 mV		VTT_dc + 75 mV	5, 6
VDDA	VDDA Supply Voltage	V	2.4	2.5	2.6	
IDDIO1	VDDIO Power Supply Current	A			3.6	3, 9
IDDIO2	VDDIO Power Supply Current in S3 State	mA			120	
ITT1	VTT Power Supply Current	A			1.75	2, 4, 9
ITT2	VTT Power Supply Current in S3 State	mA		0		
ILDT	VLDT Power Supply Current	mA			500	1, 9
IDDA	VDDA Power Supply Current	mA			250	9

Notes:

1) ILDT is specified for one 16x16-bit HyperTransport™ link operating at 2.0 GT/s.

2) VTT must both sink and source current.

3) VDDIO current is consumed by I, O, I/O switching current and on-chip functions (PDL, DLL, level-shifters, etc.).

4) VTT current is consumed by I, O, I/O switching current and on-chip functions (PDL, DLL, level-shifters, etc.).

5) VDDIO_ac and VTT_ac parameters are measured over 60 seconds time frame with all data bus bits switching.

6) Power supply A/C measurements use a 20-MHz scope bandwidth limit.

7) All voltages are referenced to VSS. In order to ensure proper functionality, DC voltage regulator must be set accordingly to ensure that VDDIO_dc level measured at the VDDIO_FB_H/L pins does not exceed the specified maximum and minimum range. As such, factors such as voltage regulator inaccuracy and IR drop must be carefully considered and compensated for. For example, if the inaccuracy and IR drop amounts to 50 mV, then the voltage regulator setting for VDDIO should not be lower than 1.75 V to avoid violating the VDDIO_dc minimum spec of 1.7 V.

*8) All voltages are referenced to VSS. Voltage regulator for VTT must be set accordingly so that VTT_dc level measured at the processor VTT_SENSE pin tracks 0.5*VDDIO_dc and stays within the specified maximum and minimum range. Factors such as voltage regulator inaccuracy and IR drop must be carefully considered and compensated for. For example, if the inaccuracy and IR drop amounts to 20 mV, the voltage regulator setting has to be set 20 mV higher so that VTT still tracks 0.5*VDDIO_dc and stays within the range of 0.85 V and 0.95 V.*

9) This specification reflects the values published in the appropriate power roadmap document.

7.2 bbpmmmm **H** vtcdd - **Socket S1 Power Supply Operating Conditions**

Table 44. bbpmmmm **H** vtcdd **VDD Power Supply DC Operating Conditions**

Symbol	Parameter	Units	Min	Typ	Max	Notes
VID_VDD	VID Requested VDD Supply Level	V	Refer to the thermal/power and BIOS tables under the appropriate SOPN section for this OPN specific parameter.			1
VDD_lps	VDD Supply Voltage in the lowest frequency P-state (minimum P-state)	V	VID_VDD – 25 mV	VID_VDD	VID_VDD + 25 mV	
VDD_ips	VDD Supply Voltage in all intermediate frequency P-states	V	VID_VDD – 25 mV	VID_VDD	VID_VDD + 55 mV	
VDD_hps	VDD Supply Voltage in the highest frequency P-state (maximum P-state)	V	VID_VDD – 25 mV	VID_VDD	VID_VDD + 55 mV	
VDD_PON	VDD Supply Voltage before PWROK assertion during power-on.	V	1.050 V	1.100 V	MaxVID	2, 3
IDD	VDD Power Supply Current	A	Refer to the thermal/power tables under the appropriate SOPN section for this OPN specific parameter.			

Notes:
1) The processor drives a VID code corresponding to this voltage.
2) The processor's VID[5:0] outputs select VDD_PON nom before PWROK is asserted. Transients up to MaxVID are allowed.
3) MaxVID is reported in MSRC001_0042 (FIDVID_STATUS).

Table 45. bbpmmmm **H** vtcdd **VDD Power Supply AC Operating Conditions**

Symbol	Parameter	Units	Min	Typ	Max	Notes
VDD_ac	VDD Supply Voltage	V	VID_VDD – 125 mV		VID_VDD + 125 mV	1

Notes:
1) Transient duration below VDD_dc min is limited to <5 µs. Transient duration above VDD_dc max is limited to <100us and <50% duty cycle. Test by probing differentially the processor's VDD_FB_H/L signals using a 20 MHz scope bandwidth limit.

Table 46. bbpmmmm **H** vtcdd **Non-VDD Power Supply AC and DC Operating Conditions**

Symbol	Parameter	Units	Min	Typ	Max	Notes
VDDIO_dc	VDDIO Supply Voltage for DDR2 electricals	V	1.7	1.8	1.9	7
VDDIO_ac	VDDIO supply voltage	V	VDDIO_dc – 150 mV		VDDIO_dc + 150 mV	5, 6
VLDT	VLDT Supply Voltage	V	1.14	1.2	1.26	
VTT_dc	VTT Supply Voltage for DDR2 electricals	V	0.85	0.9	0.95	8
VTT_ac	VTT Supply Voltage	V	VTT_dc – 75 mV		VTT_dc + 75 mV	5, 6
VDDA	VDDA Supply Voltage	V	2.4	2.5	2.6	
IDDIO1	VDDIO Power Supply Current	A			3.6	3, 9
IDDIO2	VDDIO Power Supply Current in S3 State	mA			120	
ITT1	VTT Power Supply Current	A			1.75	2, 4, 9
ITT2	VTT Power Supply Current in S3 State	mA		0		
ILDT	VLDT Power Supply Current	mA			500	1, 9
IDDA	VDDA Power Supply Current	mA			40	9

Notes:

1) ILDT is specified for one 16x16-bit HyperTransport™ link operating at 1.6 GT/s.

2) VTT must both sink and source current.

3) VDDIO current is consumed by I, O, I/O switching current and on-chip functions (PDL, DLL, level-shifters, etc.).

4) VTT current is consumed by I, O, I/O switching current and on-chip functions (PDL, DLL, level-shifters, etc.).

5) VDDIO_ac and VTT_ac parameters are measured over 60 seconds time frame with all data bus bits switching.

6) Power supply A/C measurements use a 20-MHz scope bandwidth limit.

7) All voltages are referenced to VSS. In order to ensure proper functionality, DC voltage regulator must be set accordingly to ensure that VDDIO_dc level measured at the VDDIO_FB_H/L pins does not exceed the specified maximum and minimum range. As such, factors such as voltage regulator inaccuracy and IR drop must be carefully considered and compensated for. For example, if the inaccuracy and IR drop amounts to 50 mV, then the voltage regulator setting for VDDIO should not be lower than 1.75 V to avoid violating the VDDIO_dc minimum spec of 1.7 V.

*8) All voltages are referenced to VSS. Voltage regulator for VTT must be set accordingly so that VTT_dc level measured at the processor VTT_SENSE pin tracks 0.5*VDDIO_dc, and stays within the specified maximum and minimum range. Factors such as voltage regulator inaccuracy and IR drop have to be carefully considered and compensated for. For example, if the inaccuracy and IR drop amounts to 20 mV, the voltage regulator setting must be set 20 mV higher so that VTT still tracks 0.5*VDDIO_dc and stays within the range of 0.85 V and 0.95 V.*

9) This specification reflects the values published in the appropriate power roadmap document.

8 Power Limit Encoding

The power limit is encoded in the BrandID field returned by the CPUID instruction (CPUID Fn8000_0001 EBX[8:6,14] = PwrLmt[3:0]). The following tables specify the unique encodings for PwrLmt[3:0] by socket compatibility and dual-core capability (CmpCap). The PwrLmt[3:0] encoding is used by BIOS for optional features. For details on BIOS usage of the power limit encoding, refer to the *BIOS and Kernel Developer's Guide for AMD NPT Family 0Fh Processors,* order #32559. The PwrLmt[3:0] encoding should not be used for thermal design purposes.

Socket compatibility and dual-core capability (CmpCap) must be used in conjunction with the PwrLmt[3:0] encoding to determine the associated power limit. Table 47 defines the socket compatibility encodings and Table 48 defines the dual-core capability (CmpCap) encodings.

Table 47. Socket Compatibility Encodings

Socket	Encoding
Socket AM2	11b
Socket S1	00b

Table 48. Dual-Core Capability (CmpCap) Encodings

CmpCap	Encoding
Single-Core	00b
Dual-Core	01b

Table 49. Socket AM2 Processor Power Limit Encoding

OPN Character	Power Limit	PwrLmt[3:0]
A	62 W	8h (CmpCap = 00b)
A	89 W	8h (CmpCap = 01b)
A	103 W	Ah (CmpCap = 01b)
A	125 W	Ch (CmpCap = 01b)
D	35 W	4h (CmpCap = 00b)
D	35 W	2h (CmpCap = 01b)
H	45 W	5h (CmpCap = 00b)
I	76 W	7h (CmpCap = 01b)
O	65 W	6h (CmpCap = 01b)
X	125 W	Ch (CmpCap = 01b)
N	62 W	4h (CmpCap = 01b)

Table 50. Socket S1g1 Processor Power Limit Encoding

OPN Character	Power Limit	PwrLmt[3:0]
S	25 W	6h (CmpCap = 00b)
F	8 W	1h (CmpCap = 00b)
C	9 W	2h (CmpCap = 00b)
D	35 W	Ch (CmpCap = 00b)
D	35 W	Ch (CmpCap = 01b)

9 MTOPS

Table 51 shows the Composite Theoretical Performance (CTP) calculations ("Calculations") for the Mobile AMD Sempron™ processor, AMD Turion™ 64 X2 Mobile Technology and Mobile AMD Athlon™ 64 X2 Dual-Core processor. The Calculations are stated in Millions of Theoretical Operations Per Second (MTOPS) and are based upon a formula in the United States Department of Commerce Export Administration Regulations 15 CFR 774 (Advisory Note 4 for Category 4).

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Table 51. Composite Theoretical Performance (CTP) Calculations

Frequency	MTOPS Single-Core	MTOPS Dual-Core
800	2,467	4,667
900	2,775	5,250
1000	3,084	5,834
1100	3,392	6,417
1200	3,700	7,000
1300	4,009	7,584
1400	4,317	8,167
1500	4,625	8,750
1600	4,934	9,334
1700	5,242	9,917
1800	5,550	10,500
1900	5,859	11,084
2000	6,167	11,667
2100	6,475	12,250
2200	6,784	12,834
2300	7,092	13,417
2400	7,400	14,000
2500	7,709	14,584
2600	8,017	15,167
2700	8,325	15,750
2800	8,634	16,334
2900	8,942	16,917
3000	9,250	17,500
3200	9,867	18,667

10 APP

Table 52 shows the Adjusted Peak Performance (APP) calculations ("Calculations") for the Mobile AMD Sempron™ processor, AMD Turion™ 64 X2 Mobile Technology and Mobile AMD Athlon™ 64 X2 Dual-Core processor. The Calculations are stated in Millions of Weighted Teraflops (WT) and are based upon a formula in the United States Department of Commerce Export Administration Regulations 15 CFR 774 (Advisory Note 4 for Category 4).

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Table 52. Adjusted Peak Performance (APP) Calculations

Frequency	APP Single-Core	APP Dual-Core
800	0.0005	0.0010
900	0.0005	0.0011
1000	0.0006	0.0012
1100	0.0007	0.0013
1200	0.0007	0.0014
1300	0.0008	0.0016
1400	0.0008	0.0017
1500	0.0009	0.0018
1600	0.0010	0.0019
1700	0.0010	0.0020
1800	0.0011	0.0022
1900	0.0011	0.0023
2000	0.0012	0.0024
2100	0.0013	0.0025
2200	0.0013	0.0026
2300	0.0014	0.0028
2400	0.0014	0.0029
2500	0.0015	0.0030
2600	0.0016	0.0031
2700	0.0016	0.0032
2800	0.0017	0.0034
2900	0.0017	0.0035
3000	0.0018	0.0036
3200	0.0019	0.0038